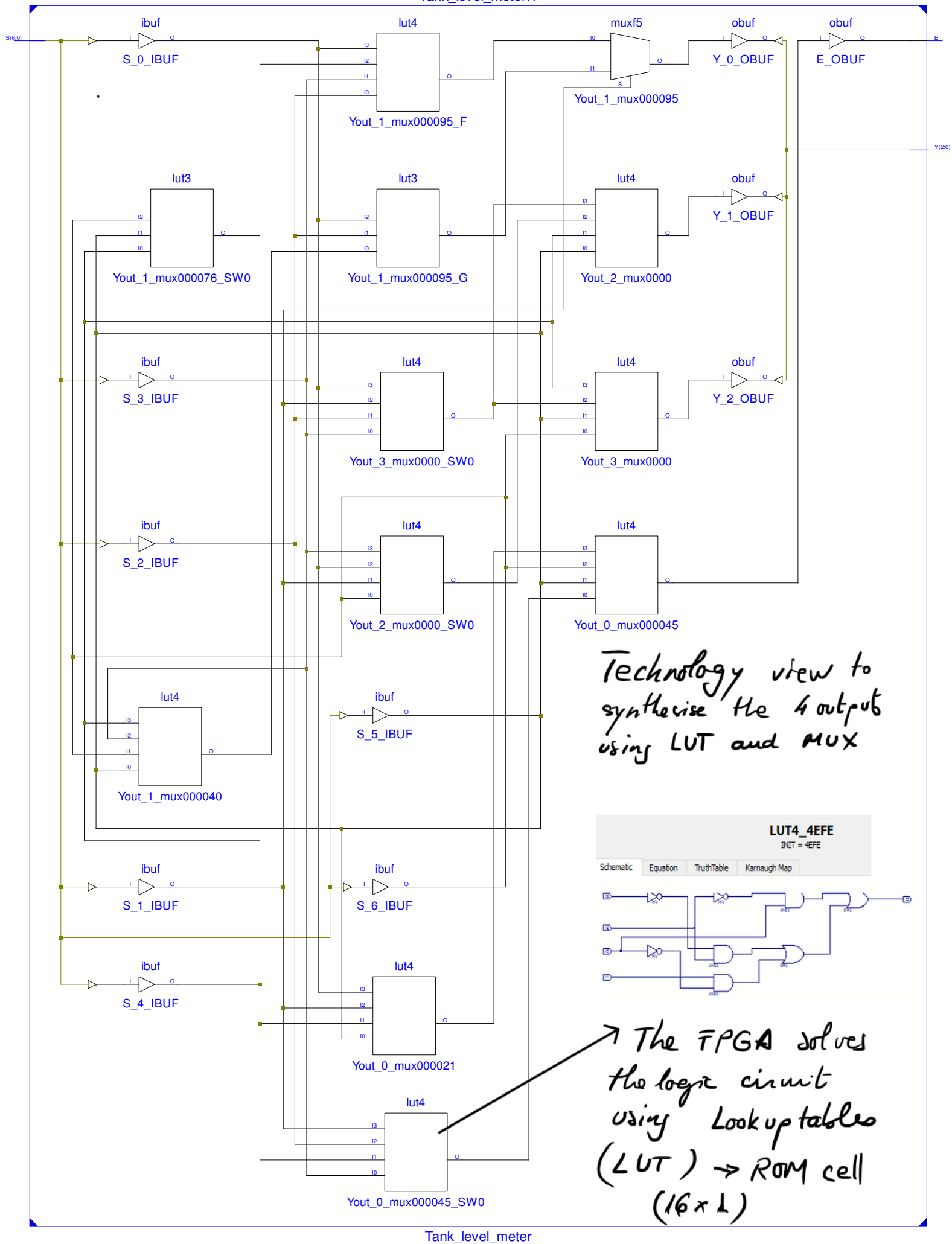

Technology view to synthesise the 4 output using LUT and MUX

The FPGA solves the logic circuit using Look up tables (LUT) → ROM cell (16 x 1)