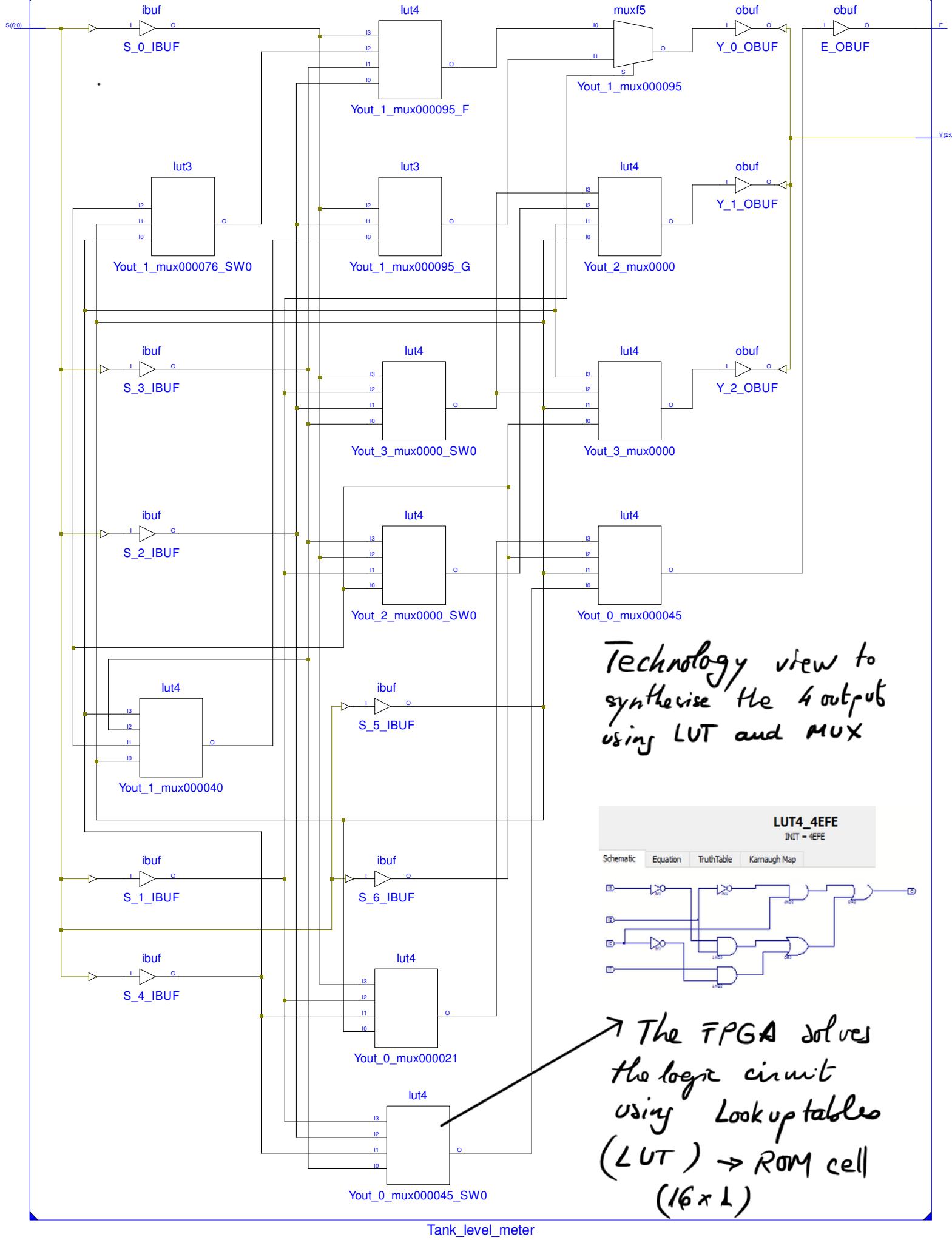
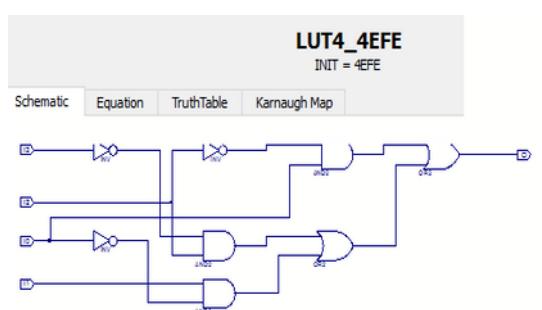


Tank_level_meter:1



Technology view to
synthesise the 4 output
using LUT and MUX



→ The FPGA solves
the logic circuit
using Lookuptables
(LUT) → ROM cell
($16 \times L$)

Tank_level_meter