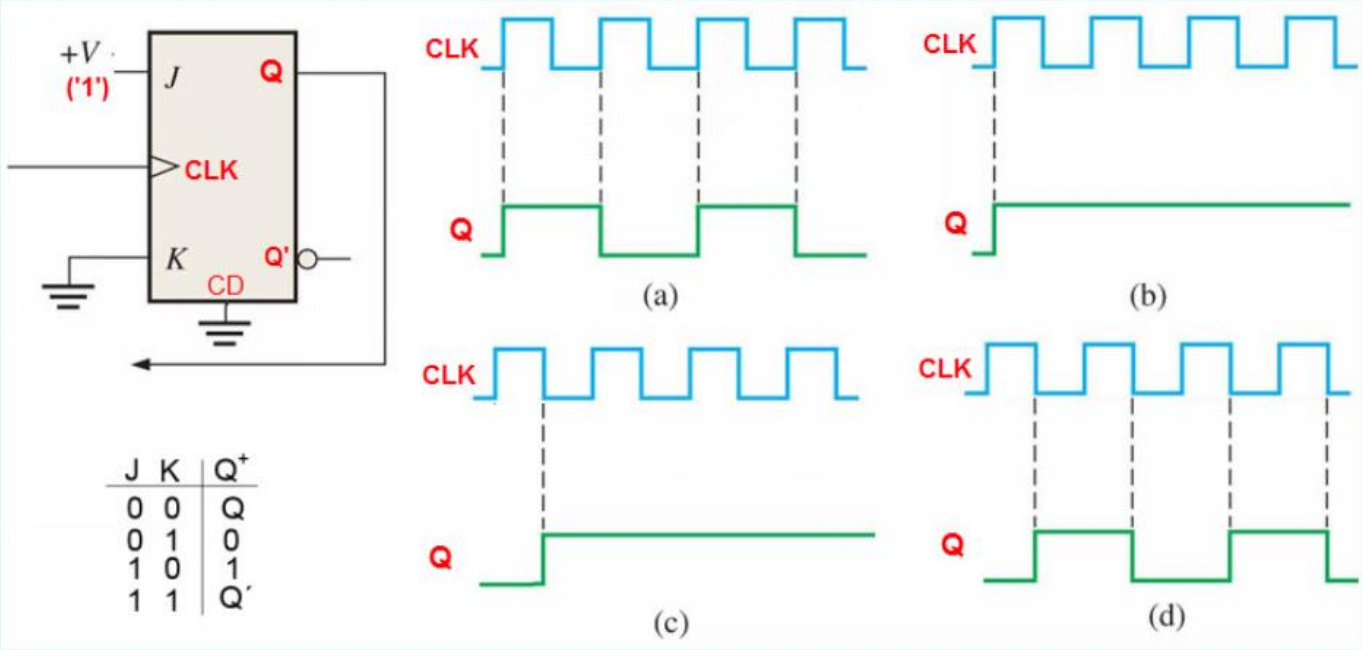
Sample P5-P6 questions

Which is the correct output of this JK flip flop connected as shown in this schematic?

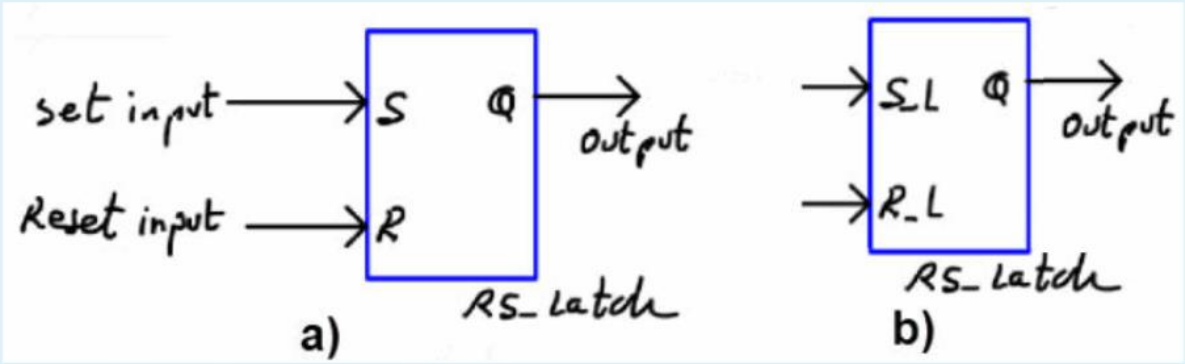


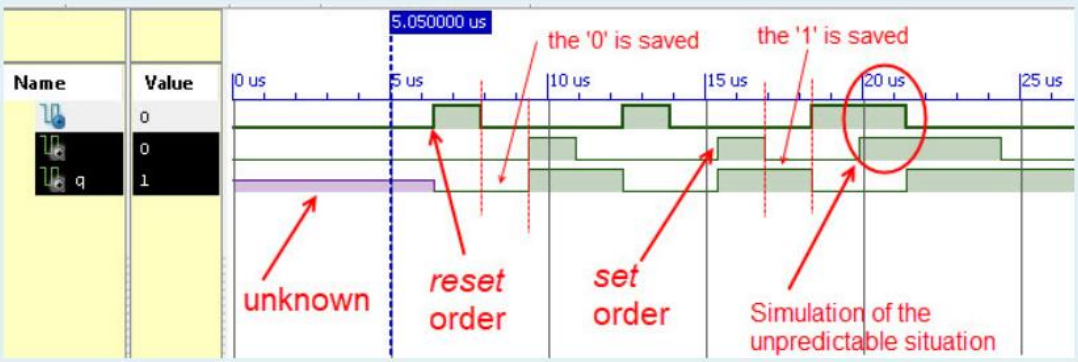
J	K	Q^+
0	0	Q
0	1	0
1	0	1
1	1	Q´

Select one:

- 1. Waveforms **d)**
- 2. Waveforms **b)**
- 3. Waveforms **c)**
- 4. Waveforms **a)**

Here we are a pair of symbols and an example of timing diagram for a 1-bit memory cell. The correct symbol that corresponds to the waveforms is the b).





Select one:

Answers

- True
- False

Examining the VHDL code below we can deduce that:

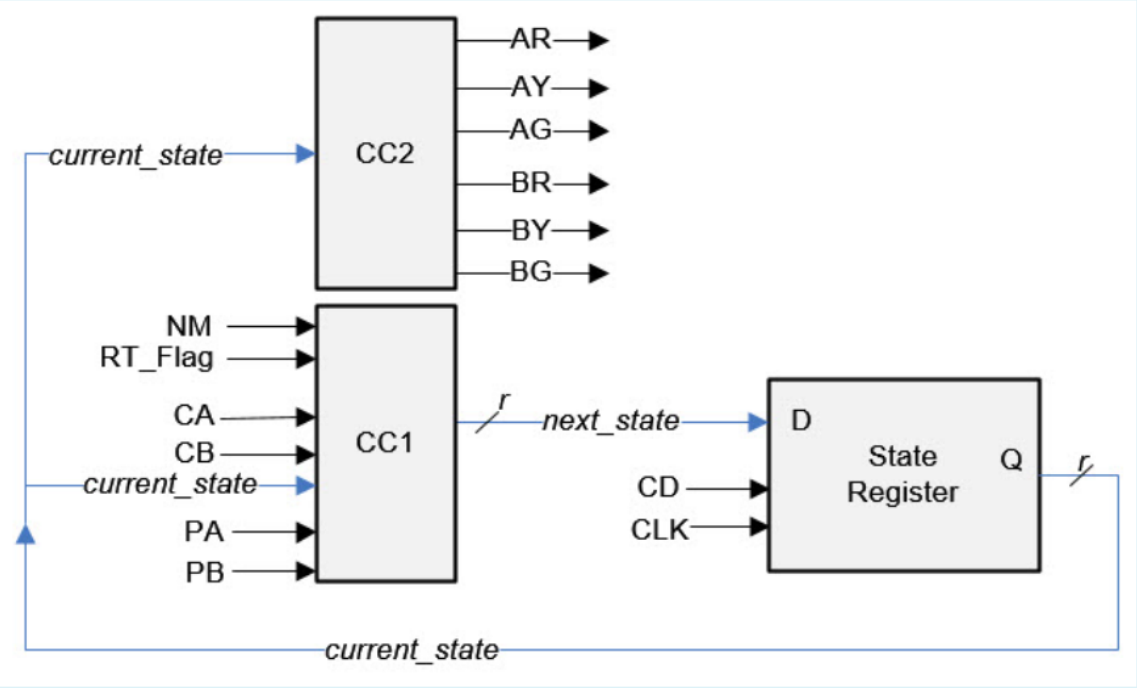
```
ARCHITECTURE structure OF circuit IS
    COMPONENT T_FF IS
        Port (
            CLK     : IN    STD_LOGIC;
            CD      : IN    STD_LOGIC;
            T       : IN    STD_LOGIC;
            Q       : OUT   STD_LOGIC
        );
    END COMPONENT;
    SIGNAL  K   : STD_LOGIC_VECTOR (3 DOWNTO 0);
BEGIN
    Chip1   : T_FF
        PORT MAP (
                CLK     => CLK,
                CD      => CD,
                T       => '1',
                Q       => K(0)
        );
    Chip2   : T_FF
        PORT MAP (
                CLK     => K(0),
                CD      => CD,
                T       => '1',
                Q       => K(1)
        );
    Chip3   : T_FF
        PORT MAP (
                CLK     => K(1),
                CD      => CD,
                T       => '1',
                Q       => K(2)
        );
    Chip4   : T_FF
        PORT MAP (
                CLK     => K(2),
                CD      => CD,
                T       => '1',
                Q       => K(3)
        );

Q  <= K;
END structure;
```

Select one:

- a. It corresponds to a synchronous circuit based on T_FF.
- b. It corresponds to an asynchronous circuit based on T_FF.
- c. Because we have no information on the entity description, we can not deduce whether the system has a common CLK for synchronicity.
- d. T_FF cannot be connected in this way, because their outputs cannot be determined.

The schematic below represents the internal architecture of a FSM to control a traffic light system. 6 outputs drive the coloured lamps and 6 inputs from several sensors and buttons determine how the machine works. The FSM has 5 states and they are coded in *one-hot*. Which one is the right answer?



Select one:

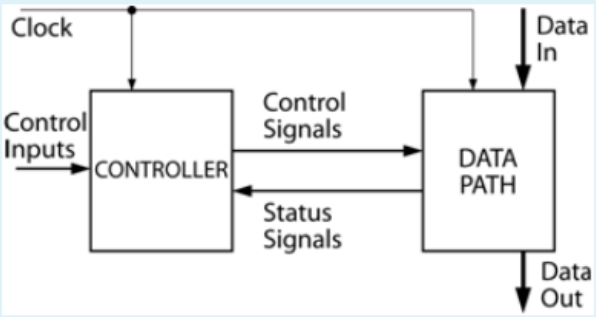
- a. It is not possible to encode the machine using *one-hot* code (00001, 00010, 00100, 01000, 10000) because binary sequential is required (000, 001, 010, 011, 100, 101).
- b. The state register contains 3 DFF; CC1 is a truth table that contains 512 combinations; CC2 has a truth table that contains 8 combinations
- c. The state register contains 5 DFF; CC1 is a truth table that contains 2048 combinations; CC2 has a truth table that contains 32 combinations.
- d. The state register contains 5 DFF; CC1 is a truth table that contains 512 combinations; CC2 has a truth table that contains 64 combinations.

CSD.

Example questions for the P7-P8 questionnaire

In datapath there are registers to save operants and results, an arithmetic and logic unit (ALU) and other combinational circuits.

The function of the status signals from the datapath to the controller FSM is to inform about the result of the operations (flags), for instance zero, carry out, negative, overflow, division by zero, etc.

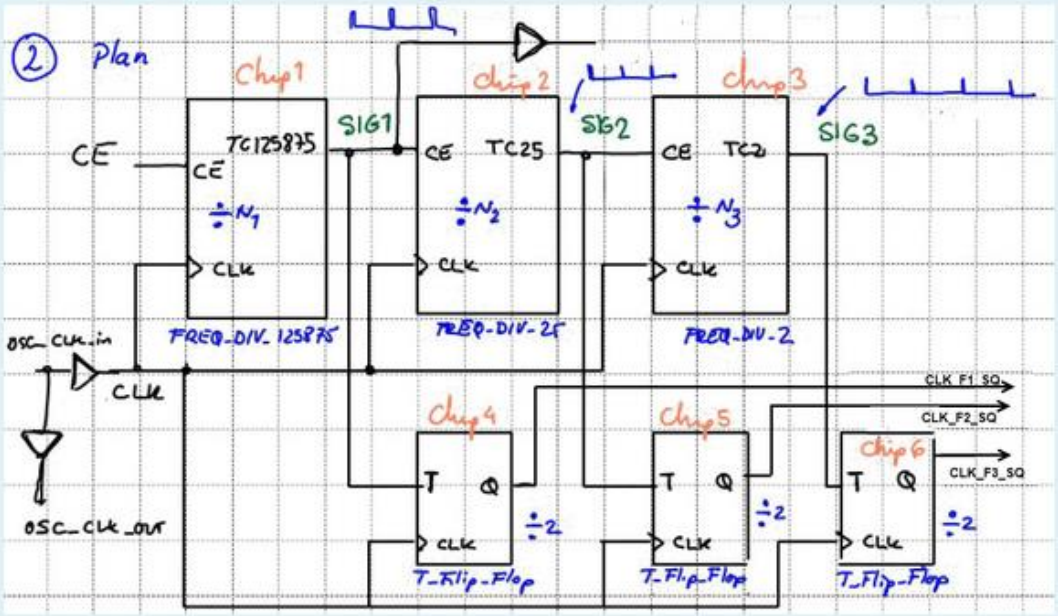


Select one:

Answers

- (•) True
- ( ) False

A *CLK_generator* circuit sketch is presented below. Which is the frequency of the output **CLK_F1_SQ** when applying an oscillator input of 100.7 MHz ?

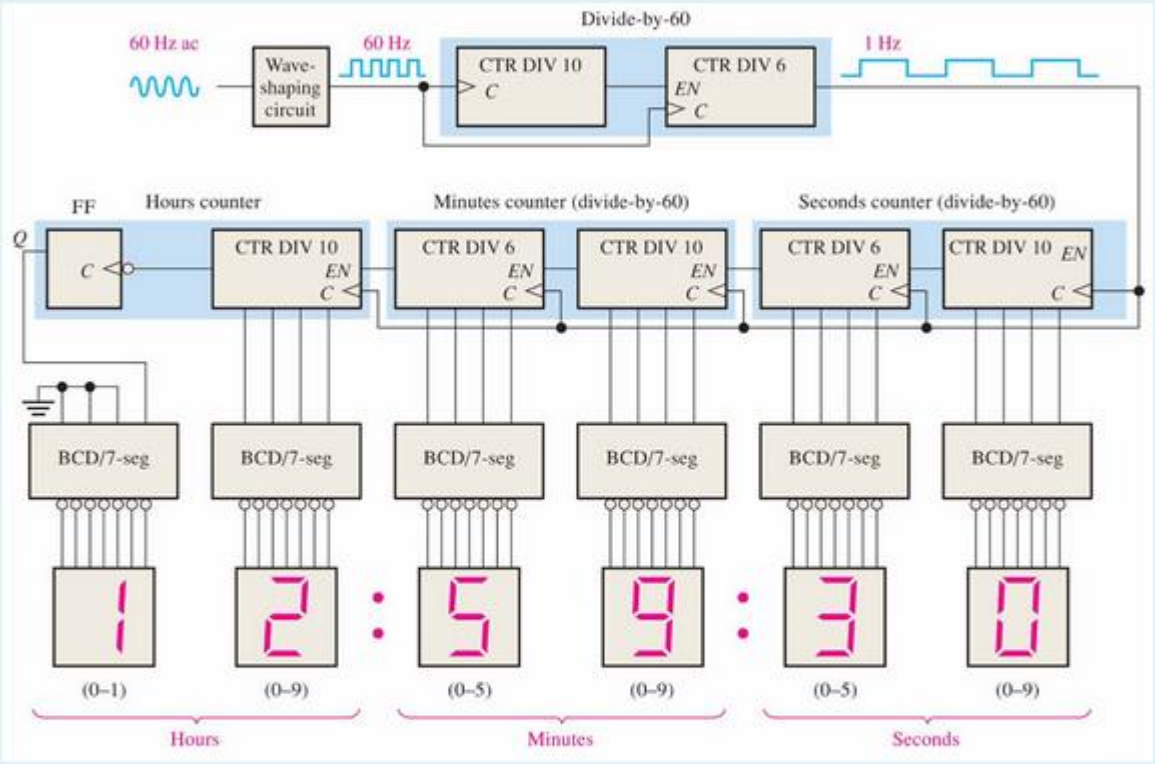


Select one:

- ( ) a. 1 Hz
- ( ) b. 25 Hz
- ( ) c. 800 Hz
- (•) d. 400 Hz

This is a schematic copied from the book T. L. Floyd, Digital Fundamentals, 9th ed., Prentice Hall, 2006. It is a design of a real-time clock that has HH:MM:SS BCD outputs. The names of the components and signals has not been adapted to our CSD naming style, but they are very similar. The wave-shaping circuit is analogue.

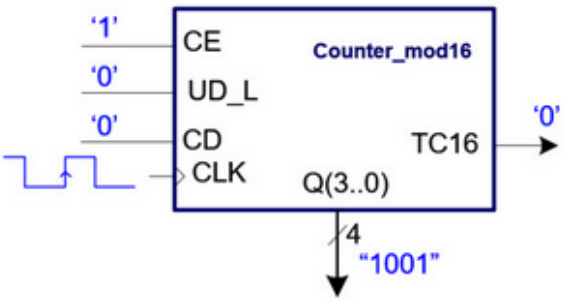
The question, after inspecting the circuit, is: how many D-FF it contains?



Select one:

- a. The circuit contains **59** data registers D-FF
- b. The circuit contains **14** data registers D-FF
- c. The circuit contains **26** data registers D-FF
- d. The circuit contains **192** data registers D-FF

With respect to the *Counter_mod16* in the picture below, which is the next state after the CLK's rising edge?



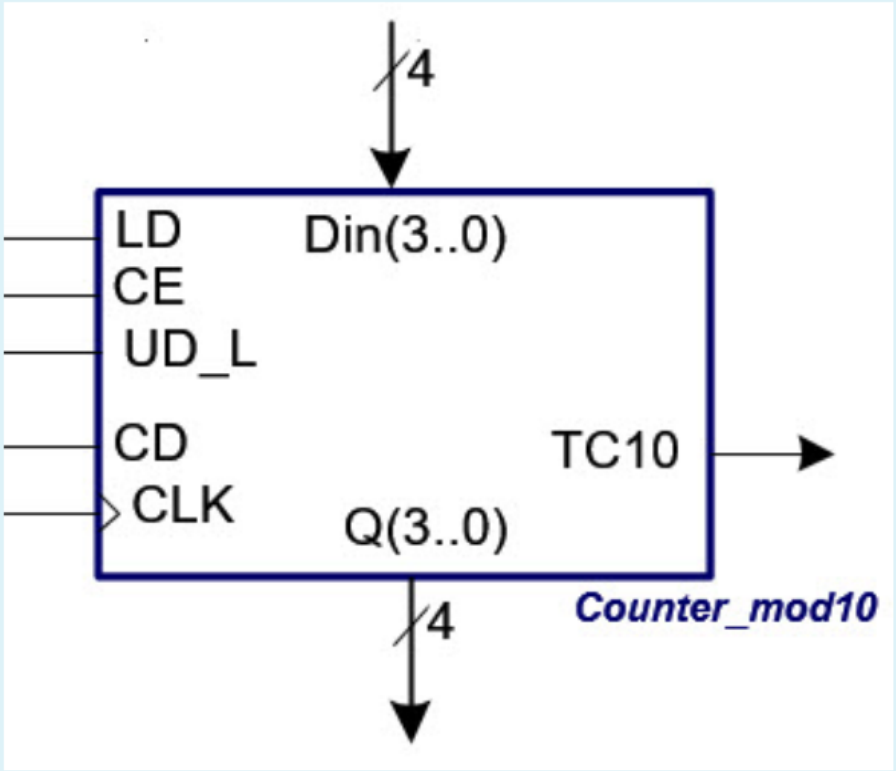
CE	UD_L	Q⁺	Synchronous operation after the CLK's rising edge
0	x	Q	Do nothing (inhibit)
1	1	$(Q+1)_{mod16}$	Up counting in binary
1	0	$(Q-1)_{mod16}$	Down counting in binary

TC16 = '**1**' when CE = '1' *and* [(Q = 15 *and* UD_L = '1') *or* (Q = 0 *and* UD_L = '0')]; '0' otherwise

Select one:

- (●) a. "1000"
- ( ) b. "1011"
- ( ) c. "1001", because the system is disabled or inhibited
- ( ) d. "1100"

Using and interconnecting 3 universal counters modulo 10 (*Counter_mod10*) like the one depicted below and other components like logic gates, we can design many different counters. Which is the maximum modulo that can be attained when connected in cascade?

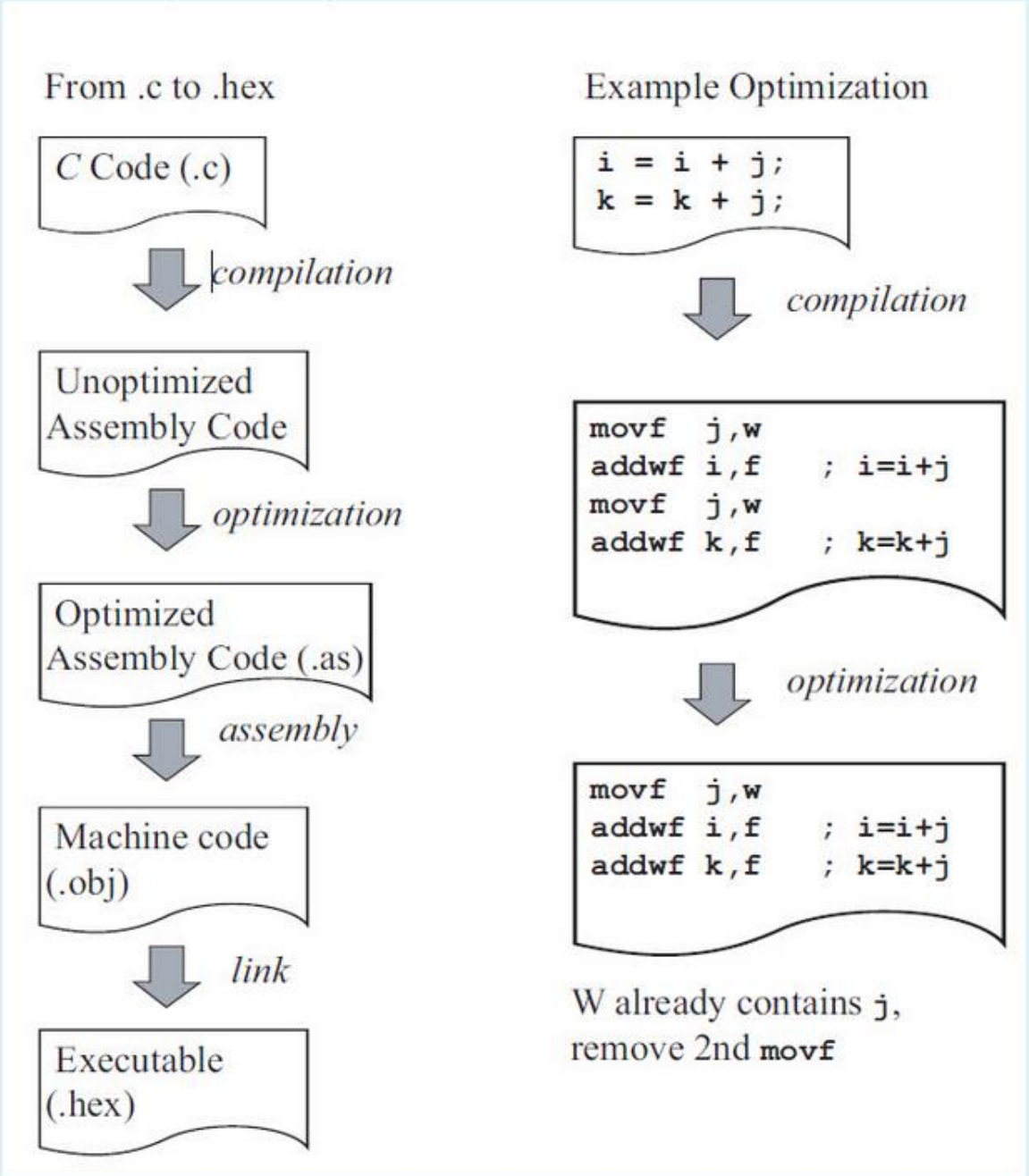


Select one:

- ( ) a. *Counter_mod100*
- (●) b. *Counter_mod1000*
- ( ) c. *Counter_mod30*
- ( ) d. *Counter_mod300*

Questionnnaire Q9_12: Example questions referring to projects P9-P10-P11-P12

C compilers allows us programming microcontroller applications skipping the inner details and complications of assembly language. However, the optimisation process as represented for example in the picture below is not for free, excepting some demonstrative versions of the compilers, because optimising is not a simple process. Typically, code size is reduced and performance improved after optimisation.



Select one:

Answers

- (•) True
- ( ) False

These are common logic bitwise operations coded in both, C and assembly languages. Name them.

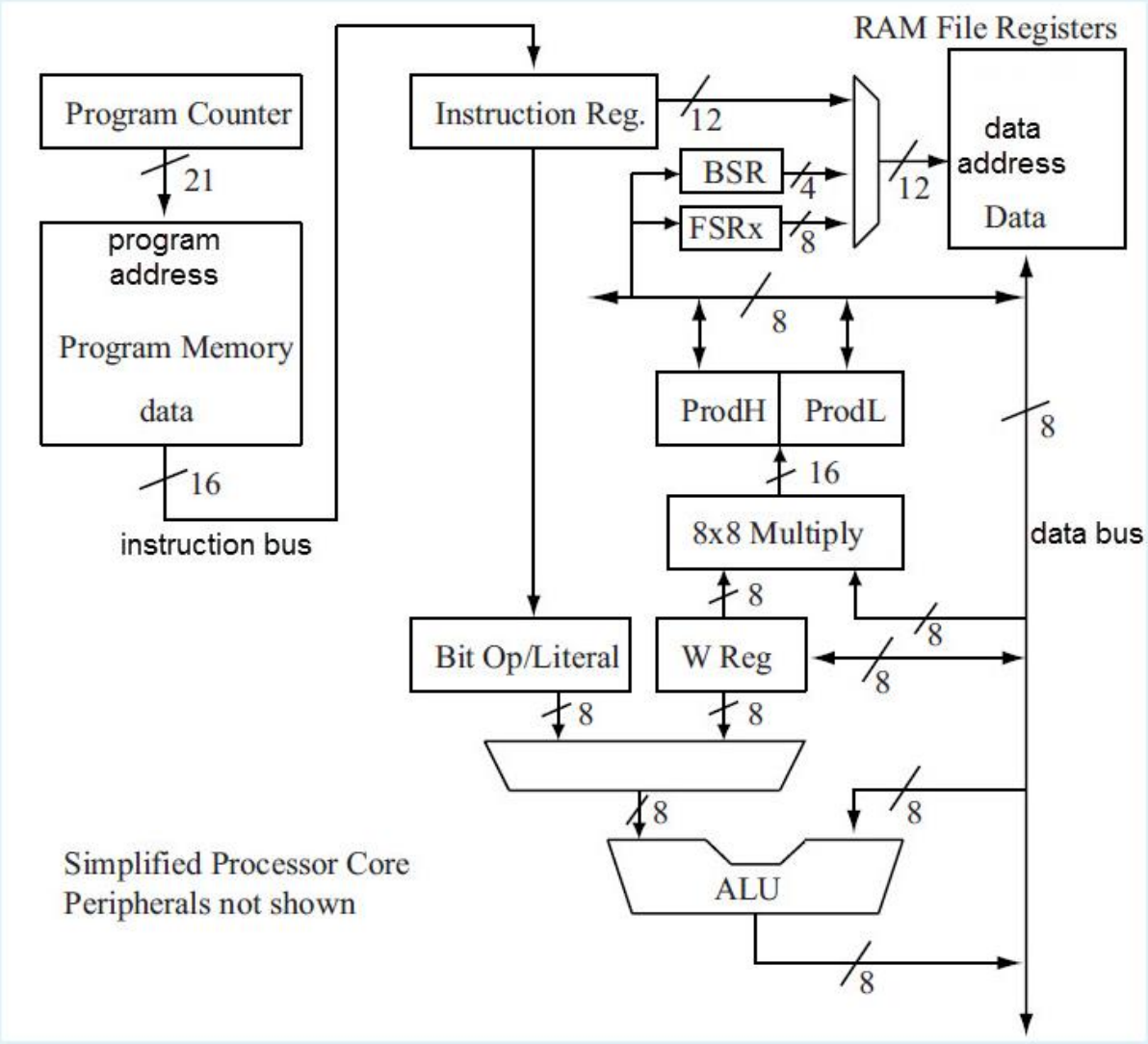
In C	In Assembly	Execution
i = i & 0x0F; **A)**	movf 0x020,w andlw 0x0F movwf 0x20	i = 0x2C = 0010 1100 &&&& &&&& mask = 0x0F = 0000 1111 --------- result = 0000 1100 = 0x0C
i = i | 0x0F; **B)**	movf 0x020,w iorlw 0x0F movwf 0x20	i = 0x2C = 0010 1100 |||| |||| mask = 0x0F = 0000 1111 --------- result = 0010 1111 = 0x2F
i = i ^ 0x0F; **C)**	movf 0x020,w xorlw 0x0F movwf 0x20	i = 0x2C = 0010 1100 ^^^^ ^^^^ mask = 0x0F = 0000 1111 --------- result = 0010 0011 = 0x23
i = ~i; **D)**	comf 0x020,f	i = 0x2C = 0010 1100 ~~~~ ~~~~ result = 1101 0011 = 0xD3

Select one:

- 1. A) AND; B) NOR; C) NXOR; D) NOT
- 2. A) AND; B) OR; C) XOR; D) NOT
- 3. A) OR; B) AND; C) NOT; D) XOR
- 4. A) AND; B) OR; C) NOT; D) XOR

Microcontrollers are characterized by having small amounts of program (flash memory) and data (RAM) memory, and take advantage of the Harvard architecture to speed processing by concurrent instruction and data access. The separate storage means the program and data memories may feature different bit widths, for example using 16-bit wide instructions and 8-bit wide data.

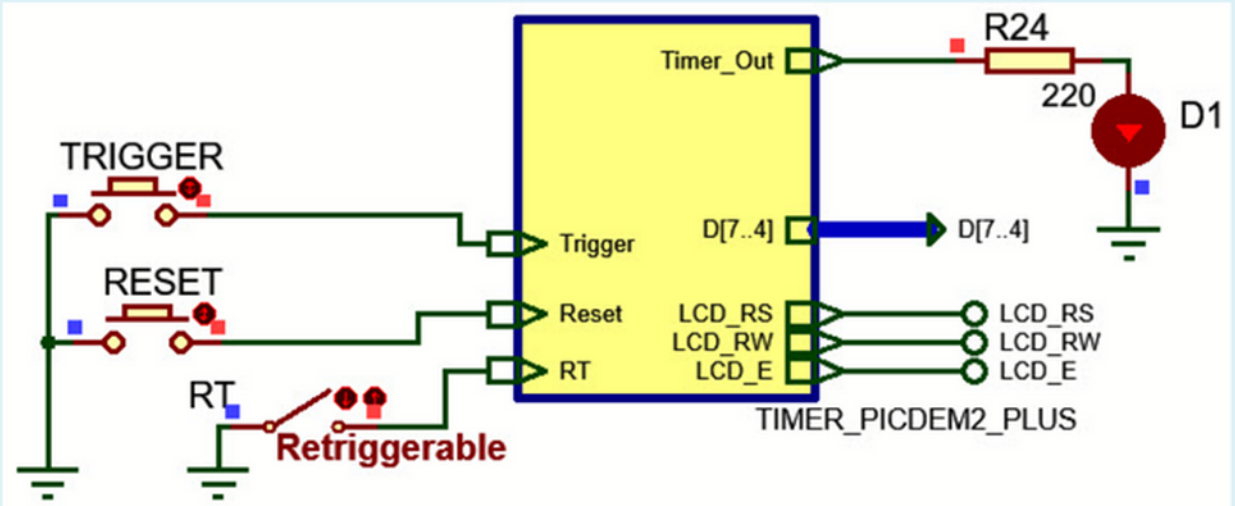
This is a simplified RTL schematic of a PIC CPU from Microchip. Which are the RAM and program memory addressing capacities?

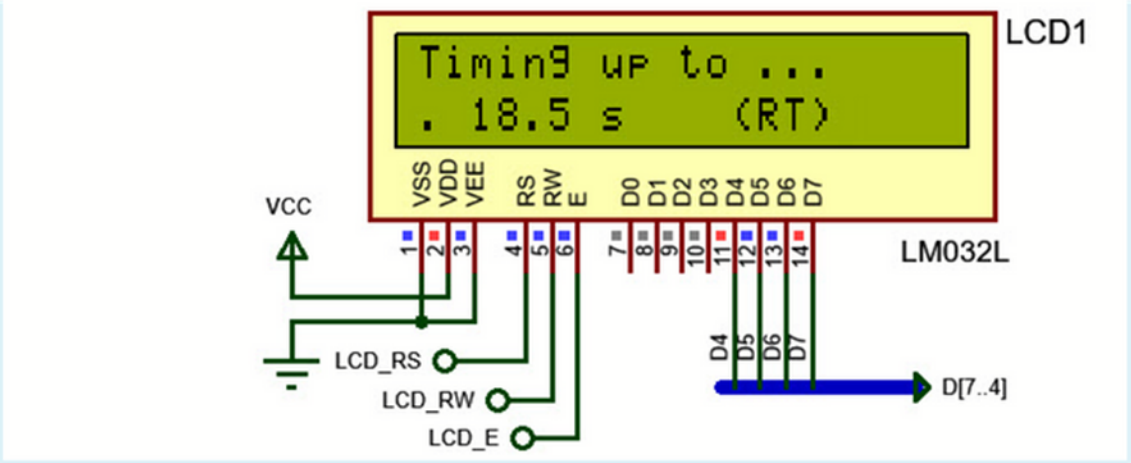


Select one:

- a. RAM memory = 4 kB (kbytes); Program memory = 2 M positions (16-bit words)
- b. RAM memory = 512 B (bytes); Program memory = 512 k positions (16-bit words)
- c. RAM memory = 1 kB (kbytes); Program memory = 1 M positions (16-bit words)
- d. RAM memory = 4 kB (kbytes); Program memory = 64 k positions (16-bit words)

This application uses the LCD board LM032L based on Hitachi HD44780 controller chip to represent ASCII messages. The code is compiled using a high level library of functions in C language, and it takes several ms to write all the characters. Which is the incorrect statement?





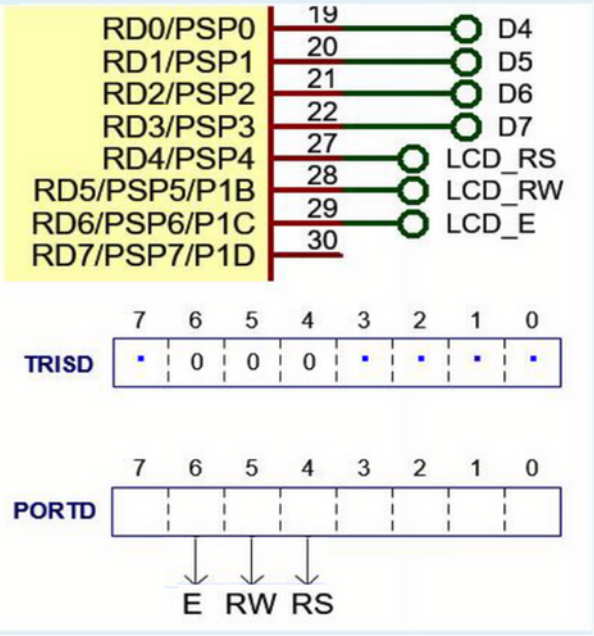
Select one:

- a. To use the LCD display efficiently, we will include the code below to write messages in the *output_logic()* function and it will be executed in every loop:

```
lcd_clear();
lcd_home();
lcd_puts("Timing up to ...");
lcd_home2();
if (Value_RT == 1)  lcd_puts (". 18.5 s    (RT)");
else lcd_puts(". 18.5 s   (nRT)")
```

- b. To compile the project without errors when using LCD functions, header files (.h) and LCD functions source files (.c) must also be included.

○ c. In order to configure the LCD hardware, the control lines RS, E, RW must be set as outputs:



Pin Functions

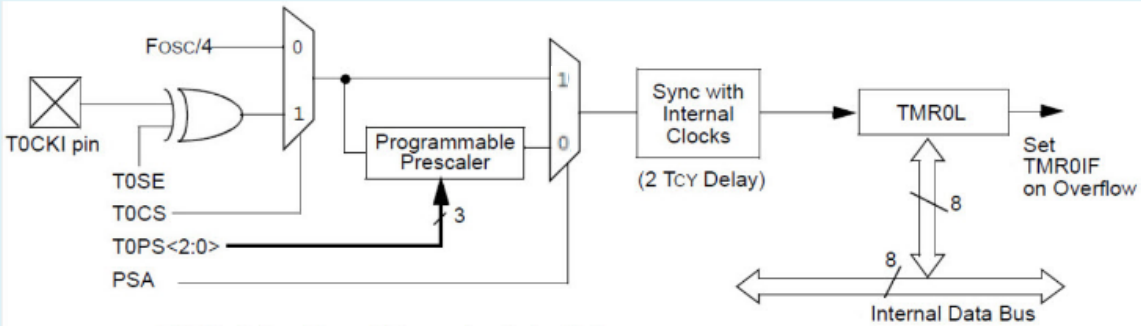
Signal	I/O	Device Interfaced with	Function
RS	I	MPU	Selects registers. 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for write and read)
R/$\overline{W}$	I	MPU	Selects read or write. 0: Write 1: Read
E	I	MPU	Starts data read/write.
DB4 to DB7	I/O	MPU	Four high order bidirectional tristate data bus pins. Used for data transfer and receive between the MPU and the HD44780U. DB7 can be used as a busy flag.
DB0 to DB3	I/O	MPU	Four low order bidirectional tristate data bus pins. Used for data transfer and receive between the MPU and the HD44780U. These pins are not used during 4-bit operation.

○ d. The *char* type variable *var_LCD_Flag* will be used to control when to write messages in the LCD: this flag will be set only when there is new information to represent on the display.

This is the PIC18F4520 Timer0 (**TMR0L**) block diagram for 8-bit mode of operation. We program the configuration bits as follows in order to use the Timer0 to measure the frequency of an external signal connected to the **T0CKI** pin:

T0SE = 0; **T0CS** = 1; **PSA** = 0; **TMR0L** = 0x00; **T0PS**(2..0) = "011"; and the Fosc = 4 MHz.

If we enable by software the Timer0 for **100 ms**, which is the maximum frequency that can be measured before there is an overflow error that invalidates the measurement?



T0PS<2:0>: Timer0 Prescaler Select bits

111 = 1:256 Prescale value
110 = 1:128 Prescale value
101 = 1:64 Prescale value
100 = 1:32 Prescale value
011 = 1:16 Prescale value
010 = 1:8 Prescale value
001 = 1:4 Prescale value
000 = 1:2 Prescale value

Select one:

○ a. $\mathbf{F}_{max} = 250\ Hz$

○ b. $\mathbf{F}_{max} = 4.096\ Hz$

○ c. $\mathbf{F}_{max} = 250\ kHz$

◉ d. $\mathbf{F}_{max} = 40.96\ kHz$