5 June 2026	UPC. EETAC. Bachelor's degree. 2A. Digital Circuits and Systems (CSD). Grades available by 9 June. Revision and corrections: 10 June, 15:00-16:00, office C4-103P	**Exam 2**

NOTE for all problems and questions: draw circuits, sketches or diagrams, explain as clearly as possible what you do and how you are inventing circuits or processing calculations as you did when you wrote your project reports. Justify your results.

Problem 1 (2p)

1. Solve the timing diagram of the circuit in Fig. 1 and deduce the sequence of numbers **Q**(2..0) generated once initialised.

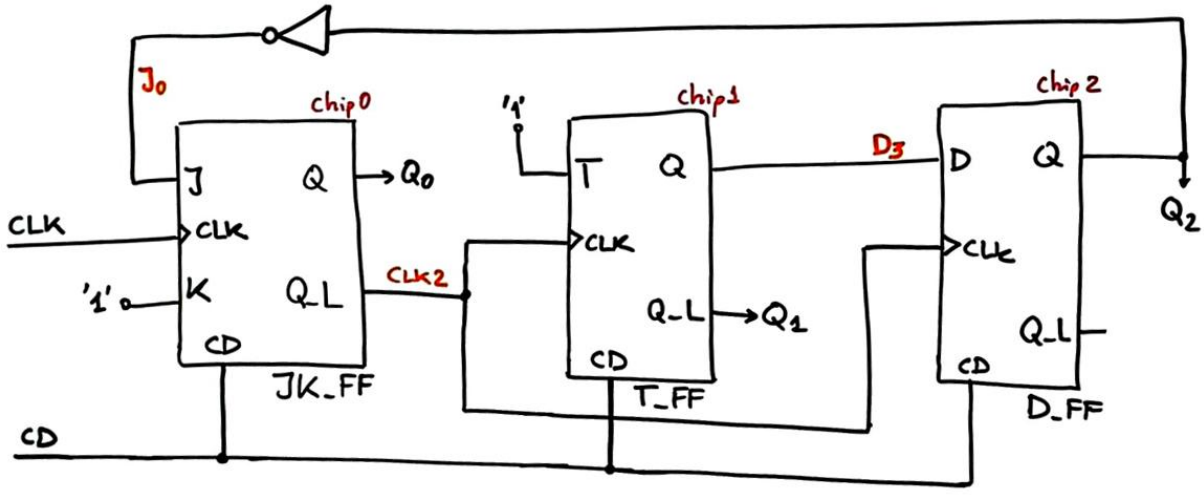


Fig. 1. Asynchronous sequential circuit.

Problem 2 (4p)

We aim to design a digital delay generator, a device similar to a timer. See Fig. 2. Once triggered by means of an **ST** signal, a single clock **Pulse** is generated after a programmable delay, consisting of *N* **CLK** clock periods (T_{CLK}).

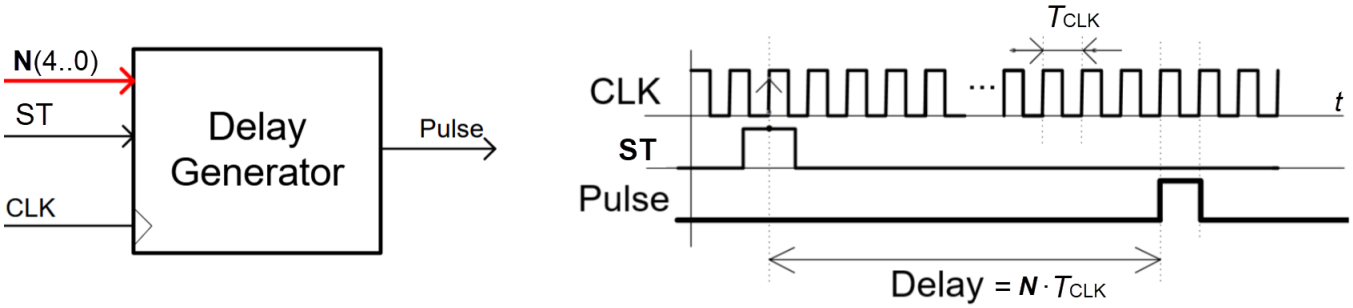


Fig. 2.

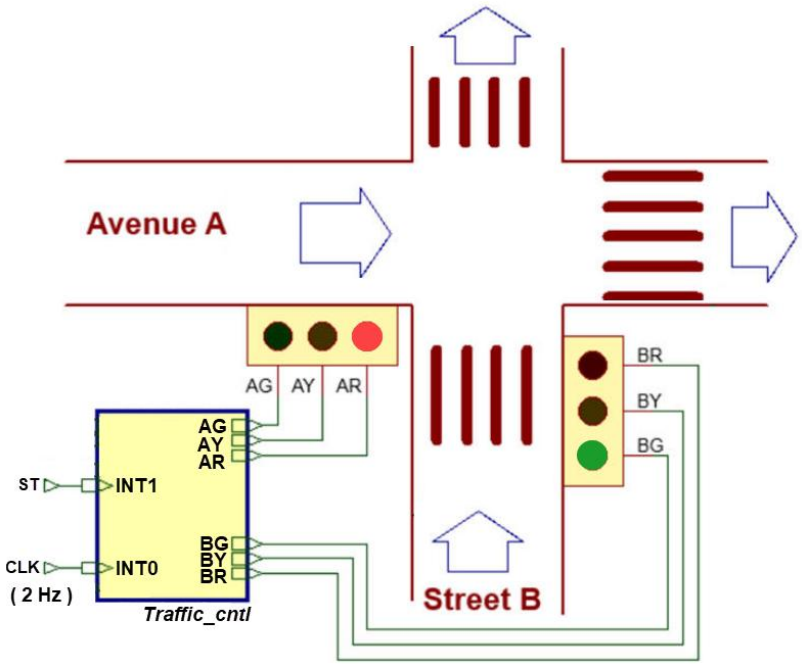
1. Propose a dedicated processor architecture for this application. Use a *Counter_mod32* in the datapath and other components if necessary.
2. Propose a state diagram for the FSM to run the application.
3. Invent the *Counter_mod32* using plan C2 and our standard *Counter_mod16* component.
4. Invent a *CLK_generator* circuit to derive three different squared **CLK** frequencies: 7.5 MHz, 25 kHz, and 1 Hz from a standard 75 MHz quartz crystal.
5. What is the time resolution of the system, referring to the minimum delay duration that can be programmed if the technology used is the CPLD Max II EPM2210F324C3 that has the following characteristics:

MAX II Device Features	EPM2210
t_{PD} (ns) gate	1.7
t_{CO} (ns)	4.6

Problem 3 (4p)

Design a basic traffic light application in two steps for the PIC18F46K22 microcontroller.
First, generate the correct sequence of lights in synchronisation with the external T_{CLK} edge for traffic light poles A and B when the **ST** push-button is pressed.
Second, set up different time durations for each colour, configuring the TMR0 peripheral.
Clicking **ST** again will stop the sequence and show this code, which blocks vehicles for both streets:

AR	AY	AG	BR	BY	BG
1	0	0	1	0	0



Traffic light sequence:

AR	AY	AG	BR	BY	BG
1	0	0	0	0	1
1	0	0	0	1	0
1	0	0	1	0	0
0	0	1	1	0	0
0	1	0	1	0	0
1	0	0	1	0	0

Fig. 3. Sketch and traffic light sequence.

1. Draw the circuit schematic. Specify port pins; include the power-on reset; and an 8 MHz quartz crystal oscillator to run the microcontroller. Explain the operations in *init_system*().
2. Draw the hardware-software diagram and propose the RAM variables.
3. Propose a state diagram for the FSM and explain how it is handled by the interrupt mechanism.
4. Fig. 4 shows the main hardware blocks of the TMR0 peripheral to be used in the second step to replace the external **CLK** signal and be able to set different time slots for each colour combination. Explain how to use it along with a software post-scaler RAM variable (**N3**) to generate, for instance, a delay of 1 minute for the green light.

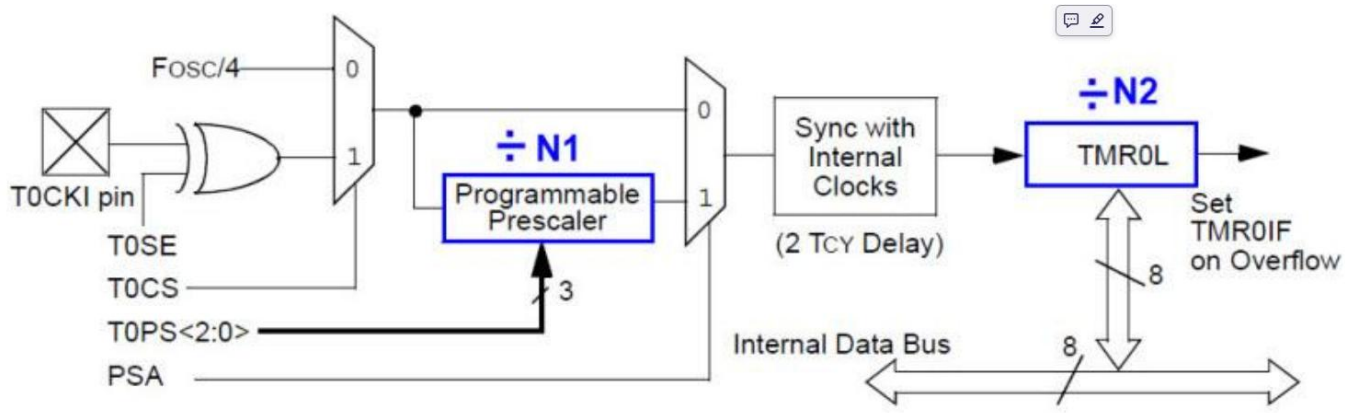


Fig. 4. TMR0 hardware from Microchip.