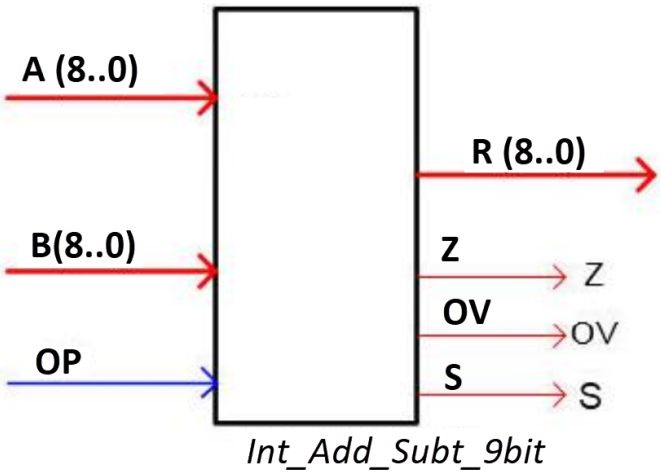
Exam 1 Grades available by 7 November. Revision and corrections: 10 November, 12:00, office C4-103P

"All unauthorised electronic devices must be turned off and kept out of students' reach. Any act of academic dishonesty, or the possession of any device or material not explicitly permitted, will result in the student being removed from the exam, receiving a grade of zero (0) for the exam, and the filing of an assessment incident report."

Problem 1 (4p)

Fig. 1 shows the symbol of a 9-bit adder/substractor that operates on integers represented in two's complement (2C).



a) **A** = (-171), **B** = 001110011, OP = 0

b) **A** = (+213), **B** = 101110011, OP = 1

Fig. 1. Combinational arithmetic operator for integer numbers.

1. Find the length of the circuit's truth table and the range of the operands and results.
2. Propose and explain an internal plan C2 architecture for the *Int_Add_Subt_9bit*. Indicate the number of VHDL files for this project.
3. If the circuit is implemented using LS-TTL technology, deduce its maximum speed. If we run gate-level simulations in ModelSim using the minimum possible *Min_Pulse* constant, how long does it take to simulate the complete truth table? Calculate the power consumption of the circuit running at its maximum speed.
4. Solve in binary 2C the operations *a*) and *b*) and find and verify the results **R**, **Z**, **OV** and **S**.

NOTE for all problems and questions: draw circuits, sketches or diagrams, explain as clearly as possible what you do and how you are inventing circuits or processing calculations as you did when you wrote your project reports. Justify your results.

Problem 2 (3p)

Fig. 2 shows the RTL view of a circuit synthesised by Altera Quartus Prime for the FPGA Cyclone IV.

1. Justify whether it is a flat or a hierarchical design. How many VHDL files does the project contain?
2. Draw the symbol and the truth table of the top entity, naming all the input and output ports. Infer how many minterms and maxterms the output **Y** has.
3. Draw the architecture of this top entity using plan A (equations) and represent the logic circuit.

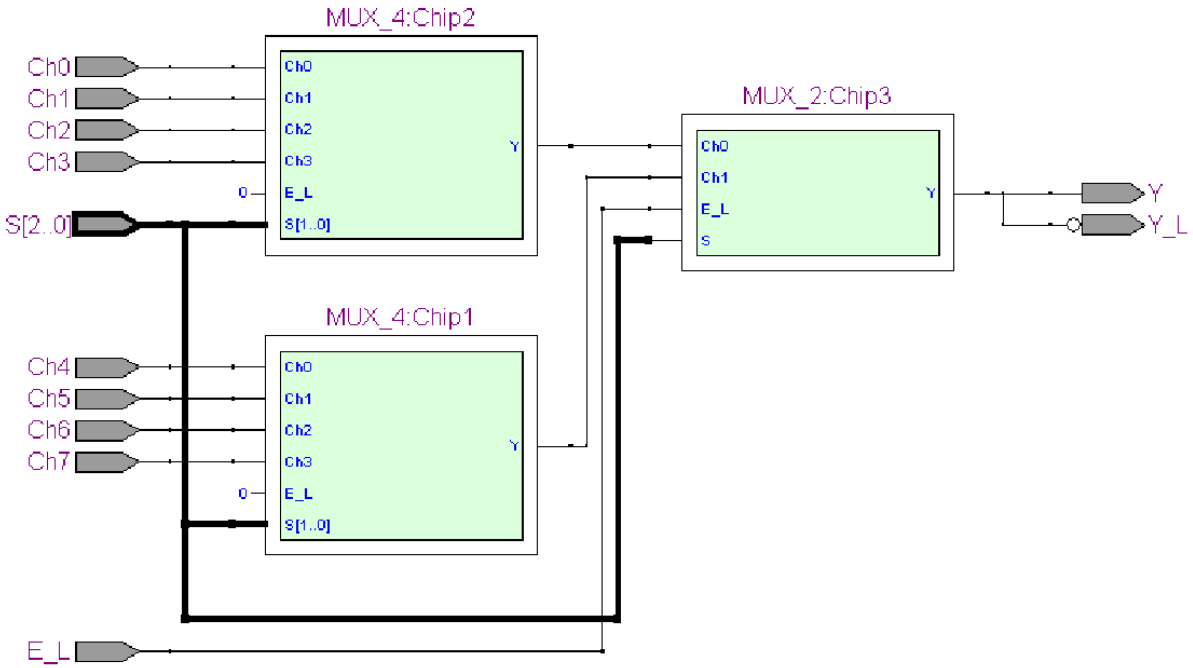


Fig. 2. RTL view schematic generated by an EDA synthesis tool for FPGA.

Problem 3 (3p)

Given de following logic function: **Y** = *f*(**A**, **B**, **C**, **D**) = **A**⊕**B** + **C**'+ **A**·**B**'·**D**

1. Draw an equivalent circuit using only 2-input NOR gates.
2. Express the function as a product of maxterms and represent its truth table.
3. Implement the logic function with the method of decoders (MoD) **or** the method of multiplexers (MoM) with a *MUX_2*.