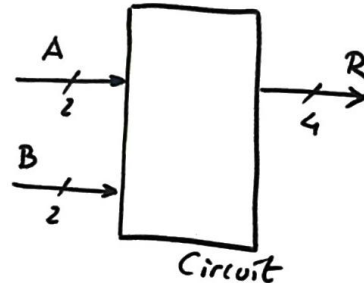


Problem 1

(3p)

1. Draw an example of timing diagram for the circuit with the truth table represented in Fig. 1. Use a *Min_Pulse* time constant of 2.32 μ s. Infer a possible application of this digital circuit.

B_1	B_0	A_1	A_0	R_3	R_2	R_1	R_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1



$$\begin{aligned}
 R_3 &= B_1 \cdot B_0 \cdot A_1 \cdot A_0 \\
 R_2 &= B_1 \cdot A_1 \cdot A_0' + B_1 \cdot B_0' \cdot A_1 \\
 R_1 &= B_0 \cdot A_1 \cdot A_0' + B_1 \cdot A_1' \cdot A_0 + B_1 \cdot B_0' \cdot A_0 + B_1' \cdot B_0 \cdot A_1 \\
 R_0 &= B_0 \cdot A_0
 \end{aligned}$$

Fig. 1. Combinational circuit and its minimised equations from Minilog.

- Express $R_2 = g(B_1, B_0, A_1, A_0)$ as a product of maxterms and $R_1 = f(B_1, B_0, A_1, A_0)$ as a sum of minterms. Draw this R_1 canonical circuit.
- From the equations in Fig. 1, implement the output R_2 using only 2-input NOR logic gates (plan A).
- Invent the *Circuit* output R_1 using the method of multiplexers (MoM) and *MUX_8* (plan C2).
- The required multiplexer *MUX_8* in the previous section 4 is built by expanding *MUX_2*, which is implemented using classic technology ALS gates (Fig. 2). Deduce and explain the *Circuit* maximum speed and its power consumption when powered at 5 V. How long does it take to complete the VHDL test bench simulation of the circuit running at maximum speed?

PARAMETER	SN74ALS04B			UNIT
	MIN	TYP	MAX	
V_{IK}			-1.2	V
V_{OH}	$V_{CC} - 2$			V
V_{OL}	0.25		0.4	V
	0.35		0.5	
I_I	0.1			mA
I_{IH}	20			μ A
I_{IL}	-0.1			mA
$I_{O\#}$	-30	-112		mA
I_{CCH}	0.65		1.1	mA
I_{CCL}	2.9		4.2	mA

	MIN	MAX	
t_{PLH}	3	11	ns
t_{PHL}	2	8	

		SN74ALS04B			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage				V
		0.8			
I_{OH}	High-level output current	-0.4			mA
I_{OL}	Low-level output current	8			mA
T_A	Operating free-air temperature	0	70		$^{\circ}$ C

$$P_S + P_{dyn} = I_{CCQ} \cdot V_{CC} + V_{CC}^2 \cdot C_L \cdot f$$

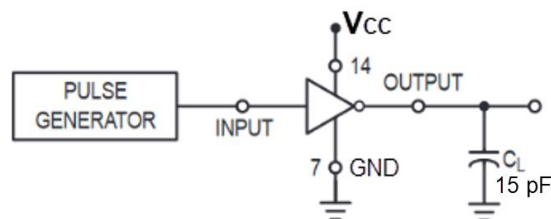


Fig. 2. Technology characteristics for the logic family ALS-TTL.

- Connect four active-low LED at the circuit's outputs and calculate their limiting resistors. Bias point: $V_{AK} = 1.9$ V, $I_{DQ} = 2.2$ mA. Draw the circuit before finding equations and calculating values.

Problem 2

(4p)

1. Draw the symbol of an *Int_add_subt_7bit* for two's complement (2C) integers. Determine the range of the operands **A**, **B** and the result **R**. Explain how the overflow (**OV**) flag works and how its circuit and truth table can be inferred. Explain the function and equation of the zero flag **Z**.
2. Fill in some truth table values performing the following integer operations in **binary**:

- | | | |
|----------------------------|---|-------------------------|
| a) (+39) | + | (1001010) _{2C} |
| b) (0010110) _{2C} | − | (-55) |
| c) (-18) | − | (1101110) _{2C} |

3. Represent the previous operations in a timing diagram and translate it (only the stimulus section) to a VHDL test bench using a constant *Min_Pulse* = 10.5 μs.
4. Invent the **plan C2** hierarchical internal schematics of the *Int_add_subt_7bit*. How many VHDL files will the project include? List all the VHDL source files and describe their functions.
5. Determine the maximum speed of operation (mops) if synthesised using classic ALS logic gates as in Fig. 2. Draw the testbench schematic and calculate how long it will take to simulate and verify all the circuit functionality.
6. Enhance the circuit in a new design phase to become an *ALU_7bit*, capable of performing integer additions, subtractions and bitwise logic AND and NOR operations, such:

- | | | |
|--------------|------------|-----------|
| d) "1010101" | NOR | "0110001" |
| e) "1010101" | AND | "0101111" |

Problem 3

(3p)

1. Apply the analysis **method I** to find the truth table of the circuit in Fig. 3. Explain specifications and planning concepts before developing the solution.

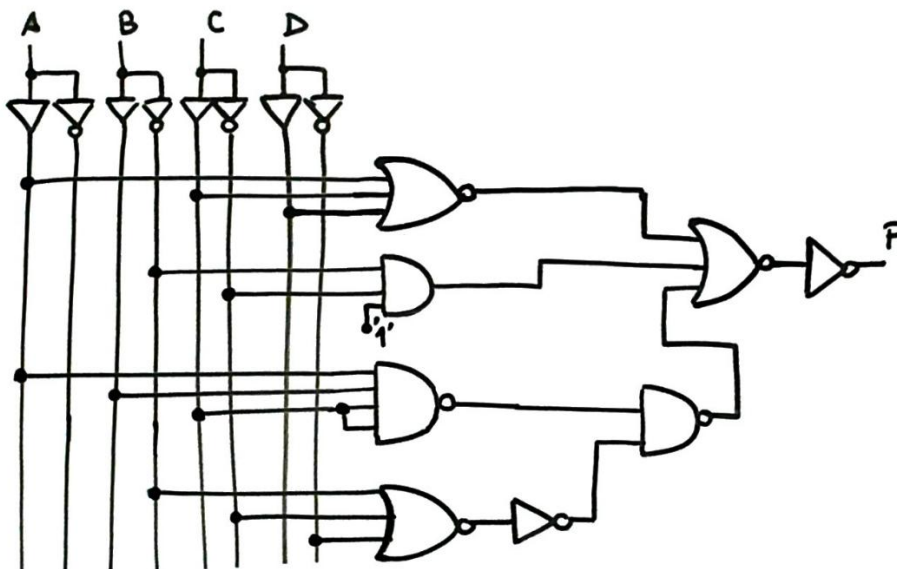


Fig. 3.

2. Explain how to find the solution to the problem using **method III** on VHDL design flow and tools.
3. Explain and plan how to design a new version of the circuit in Fig. 3 using **plan B** as the strategy to capture the truth table.

NOTE for all problems and questions: draw circuits, sketches or diagrams, explain as clearly as possible what you do and how you are inventing circuits or processing calculations as you did when you wrote your project reports. Justify your results.