UPC. EETAC. Bachelor's degree. 2A. Digital Circuits and Systems (CSD). **Exam 1.** Grades available by 4th November. Questions about exams and corrections: office time. **28th October**

Problem 1 (4p)

1. Analyse the *Circuit_T* in Fig. 1 using method I on Boole's algebra to obtain its truth table **T** = *f*(**A**, **B**, **C**, **D**).
2. We want to build a *Circuit_T* prototype in the lab, what is maximum frequency of the generator f_{MAX} that we can use to drive an input? Calculate the power consumption when the circuit is running at such frequency. Calculate both parameters for implementations using TTL_LS gates (Fig. 4).
3. Invent the truth table using a plan A based on only NOR2 gates.
4. Invent the truth table using a plan C2 based on the method of decoders (MoD). How to expand *Dec_2_4* to generate the binary decoder required in this application? How many VHDL files are required?

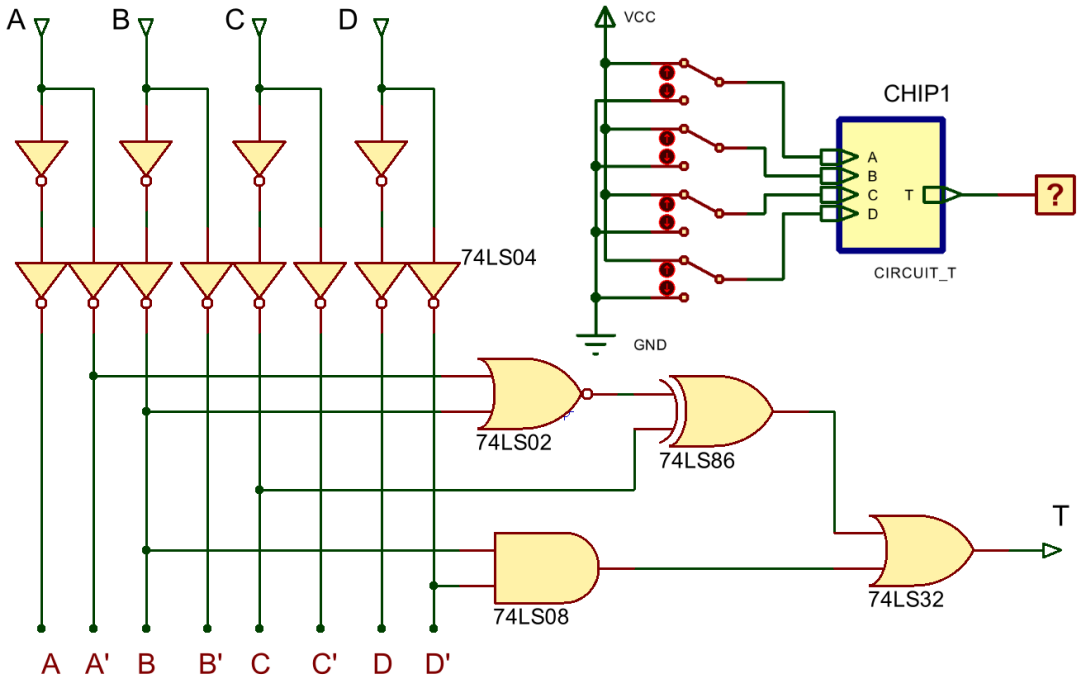

Fig. 1. Combinational circuit **T** = *f*(**A**, **B**, **C**, **D**).

Problem 2 (2p)

1. Solve the arithmetic operations below using 9-bit 2C (two's complement) binary integer number representation. Indicate when there is an overflow situation (**OV** flag). Which is operands and result range?
   a) Addition: **A** = (-216); **B** = (+125)
   b) Subtraction: **A** = (-216); **B** = (+125)
2. Draw the symbol and invent an *ALU_9bit* using plan C2 capable of performing arithmetic (additions, subtractions) and logic (AND, NOR) operations. Calculate the outputs for these vectors and complete the table below with the four operations:
   c) NOR: **A** = "101010101" ; **B** = "100110001"
   d) AND: **A** = "101010101" ; **B** = "010101111"

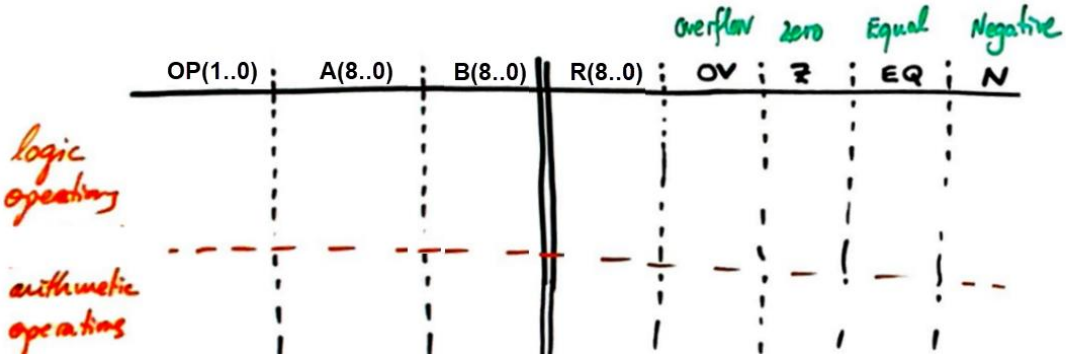

Fig. 2. Characteristics of a logic gate in LS-TTL technology.

Problem 3 (4p)

The entity represented in Fig. 3*a* is an electronic dice decoder, a combinational block for adapting the radix-2 numbers from 1 to 6 to a 7-LED display that has the typical layout shown in Fig. 3*b*. The codes **X** = "000" and **X** = "111" generate don't care outputs.

1. Deduce the circuit's truth table for all the outputs $\mathbf{L}_i = f(\mathbf{E\_L}, \mathbf{X})$ and its canonical equations.
2. As shown in the Fig. 3*a*, we connect LED active-high at each circuit output (V_{AKQ} = 1.9 V). Calculate the limiting resistors to drive each LED with I_{DQ} = 600 µA in the worst-case scenario using LS-TTL logic. Calculate the power consumption of the full circuit for the input vector: **E_L** = '0', **X** = '110'.
3. If the circuit's technology is LS-TTL, how many millions of operations per second (mops) is the circuit capable of performing? Which is the power consumption at such speed?
4. Describe the schematic or flowchart to be able to translate the truth table into VHDL using plan B. Which will be the minimum *Min_Pulse* value for ModeSim gate-level simulations?

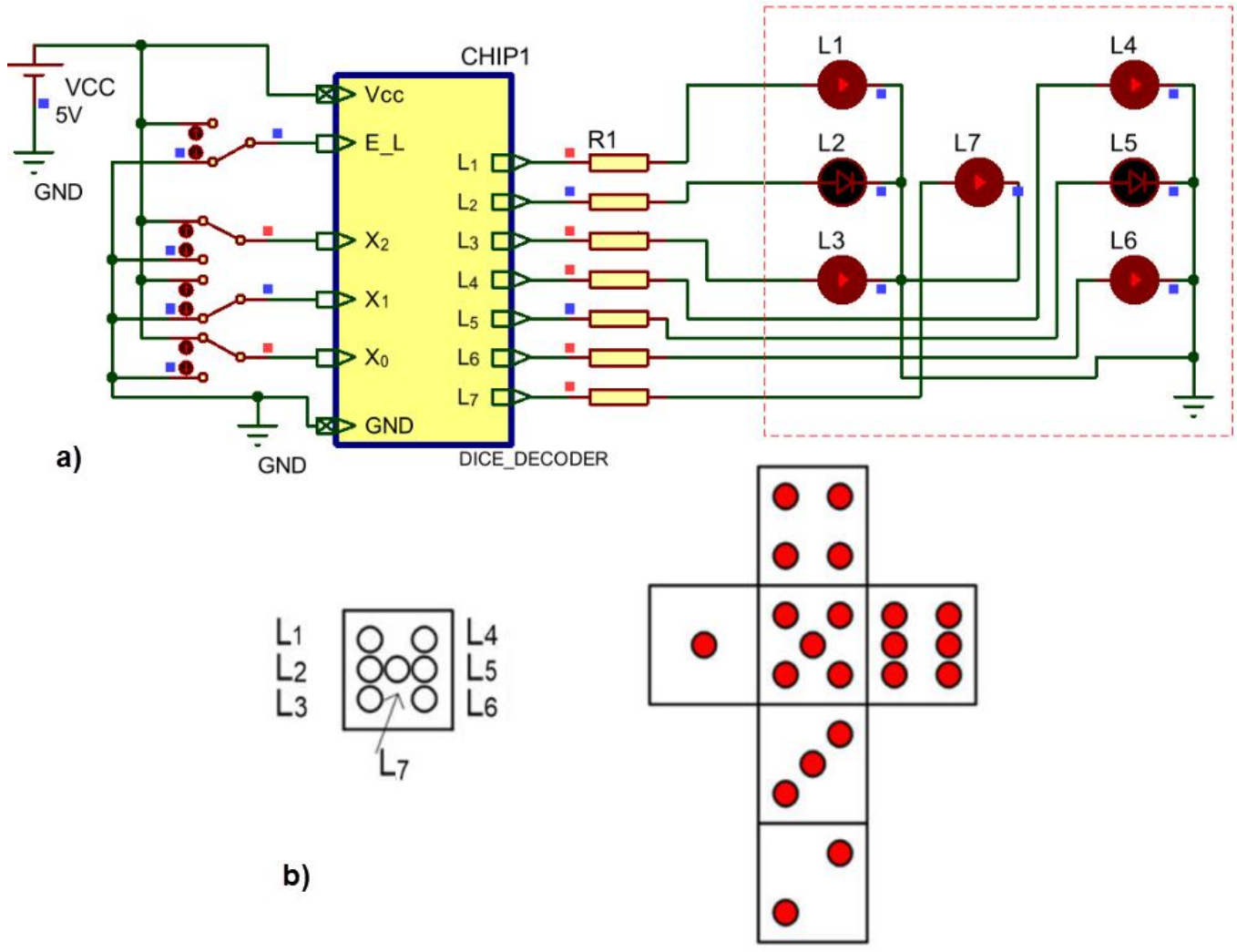

Fig. 3. *Dice_decoder* chip.

Annex. Fig. 4 shows the characteristics of a single logic gate in LS-TTL technology.

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			–0.4	mA
I_{OL}	LOW Level Output Current			8	mA

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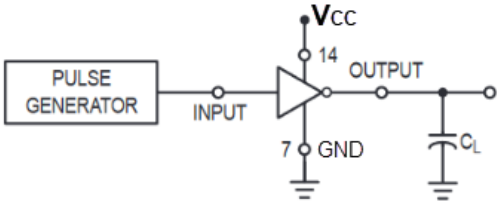
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = –18 mA			–1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			–0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	–20		–100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		1.2	2.4	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		3.6	6.6	mA

Symbol	Parameter C_L = 50 pF	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	4	15	ns



$$P_S + P_{dyn} = I_{CCQ} \cdot V_{CC} + V_{CC}^2 \cdot C_L \cdot f$$

Fig. 4. Characteristics of a logic gate in LS-TTL technology.

NOTE for all problems and questions: draw circuits, sketches or diagrams, explain as clearly as possible what you do and how you are inventing circuits or processing calculations as you did when you wrote your project reports. Justify your results.