

Problem 1

1.

$x_3 x_2 x_1 x_0$	K
0 0 0 0	1
0 0 0 1	1
0 0 1 0	0
0 0 1 1	0
0 1 0 0	1
0 1 0 1	0
0 1 1 0	X
0 1 1 1	1
1 0 0 0	0
1 0 0 1	X
1 0 1 0	0
1 0 1 1	1
1 1 0 0	X
1 1 0 1	0
1 1 1 0	X
1 1 1 1	0

$$K = m_0 + m_1 + m_4 + m_7 + m_{11} + m_{14}$$

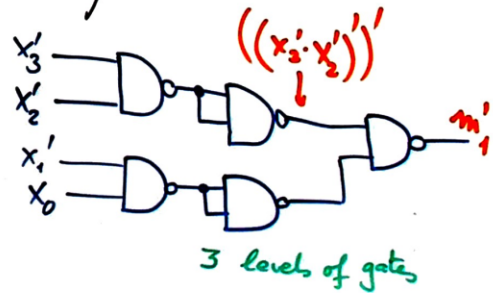
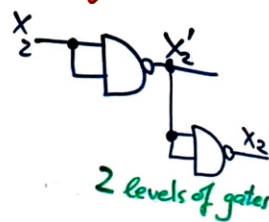
$$K = (m_0 + m_1 + m_4 + m_7 + m_{11} + m_{14})'' = (m_0' \cdot m_1' \cdot m_4' \cdot m_7' \cdot m_{11}' \cdot m_{14}')' \text{ only NAND}$$

$$K = (x_3' \cdot x_2' \cdot x_1' \cdot x_0' + x_3' \cdot x_2' \cdot x_1' \cdot x_0 + x_3' \cdot x_2 \cdot x_1' \cdot x_0' + x_3' \cdot x_2 \cdot x_1 \cdot x_0 + x_3 \cdot x_2' \cdot x_1' \cdot x_0 + x_3 \cdot x_2' \cdot x_1 \cdot x_0')$$

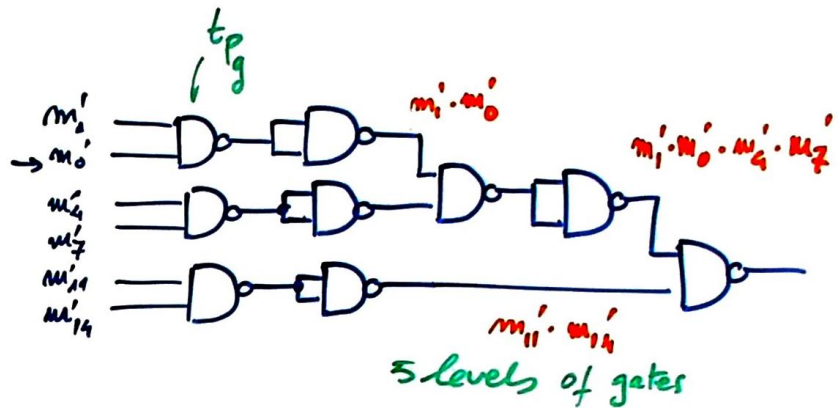
$$K = ((x_3' \cdot x_2' \cdot x_1' \cdot x_0')' \cdot (x_3' \cdot x_2' \cdot x_1' \cdot x_0)' \cdot (x_3' \cdot x_2 \cdot x_1' \cdot x_0')' \cdot (x_3' \cdot x_2 \cdot x_1 \cdot x_0)' \cdot (x_3 \cdot x_2' \cdot x_1' \cdot x_0)' \cdot (x_3 \cdot x_2' \cdot x_1 \cdot x_0'))'$$

$$m_1' = ((x_3' \cdot x_2')' \cdot (x_1' \cdot x_0'))'$$

$$m_1' = (((x_3' \cdot x_2')')' \cdot ((x_1' \cdot x_0')')')$$

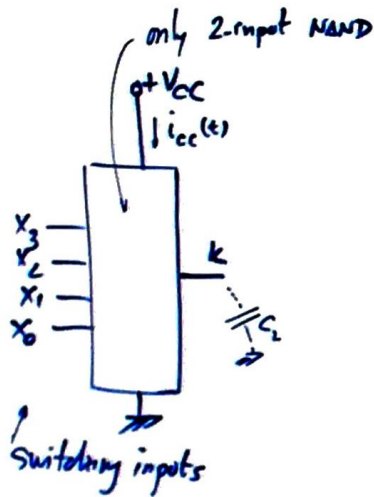


Final 6-input NAND



NGL = 5

2. We can imagine the circuit driven with stimulus that make all internal gates switching



10 gate levels

$$t_p = 10 \cdot t_{pg} = 120 \text{ ns}$$

$$P_D = V_{CC} \cdot I_{CC} + \frac{V_{DD}^2 \cdot C_L \cdot f}{P_S + P_{dyn}}$$

30

+ 8

9

47 gates

The circuit will calculate the truth table at a theoretical maximum speed $< 1/t_p = 8.3 \text{ Mops}$

• We assume all gates switch at f and all gates associated to a $C_L = C_{pd}$

For instance, an external square wave generator is driving an input at frequency f

$$f_{max} \leq \frac{1}{2 \cdot t_p} = 4.17 \text{ MHz}$$

$$P_{dyn} = 47 \cdot 5V^2 \cdot 12pF \cdot 4.17 \text{ MHz} = 58.8 \text{ mW}$$

$$P_S = 5V \cdot 20\mu A \cdot 47 = 4.7 \text{ mW}$$

number of NAND

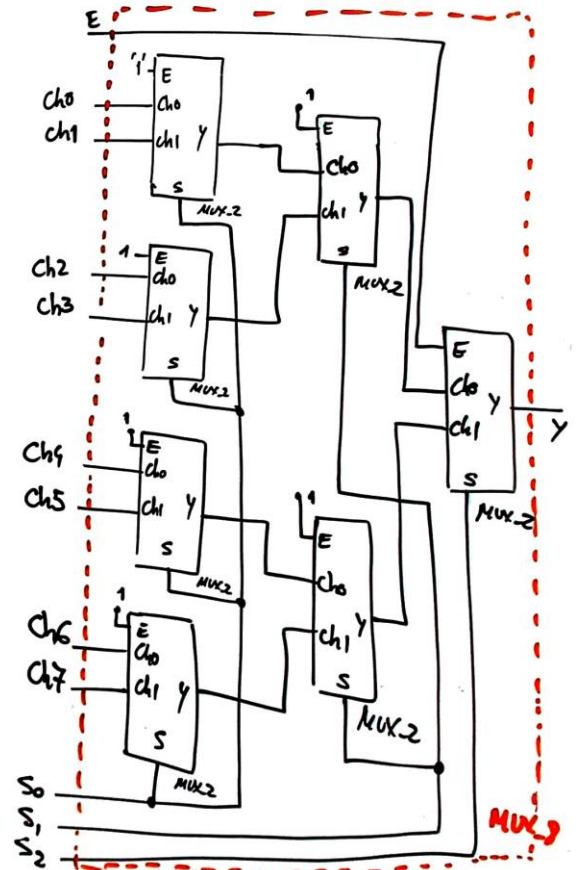
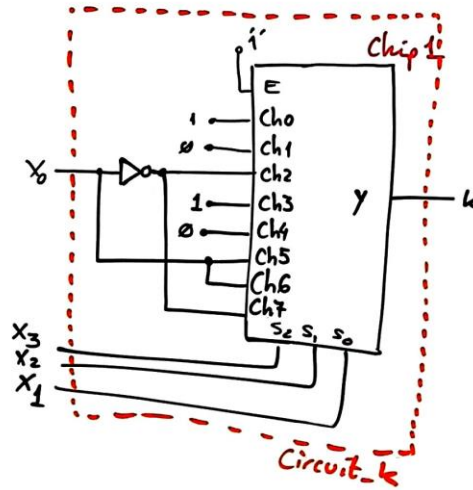
$$P_D = 63.5 \text{ mW}$$

3.

Min_Pulse minimum value for simulations or laboratory experimentation cannot be lower than t_p . If $Min_Pulse < t_p$ digital outputs are never reaching stable digital values V_{OH} and V_{OL} .

4.

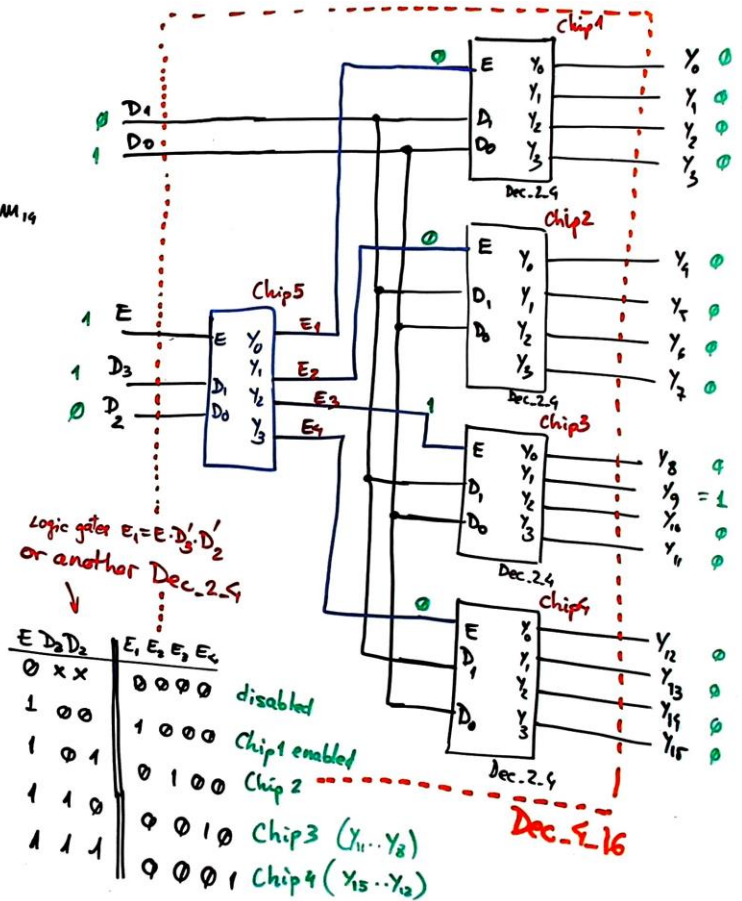
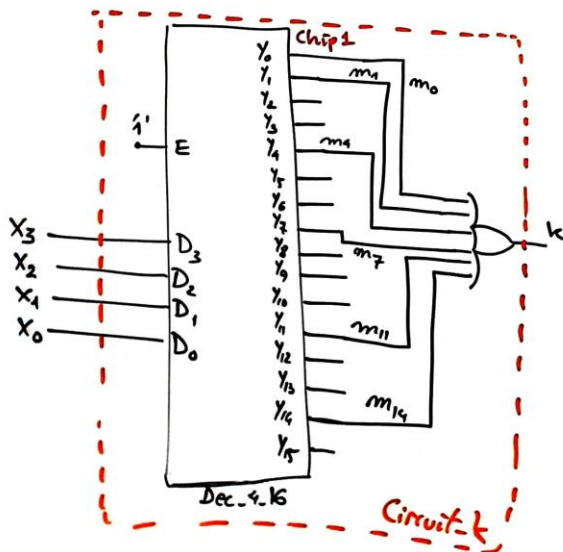
X_3	X_2	X_1	X_0	K
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	x
0	1	1	1	1
1	0	0	0	0
1	0	0	1	x
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	x
1	1	1	0	1
1	1	1	1	0



5.

Method of decoders

$$K = f(X_3, X_2, X_1, X_0) = m_0 + m_1 + m_2 + m_3 + m_{11} + m_{14}$$



Problem 2

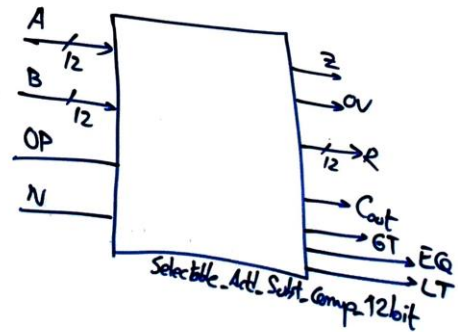
6.

When $N=0$ radix-2 numbers
 $0 \leq A, B \leq 2^{12}-1 \rightarrow 4095$
 $0 \leq [Cout, R] \leq 2^{13}-2 \rightarrow 8190$ *There is no Cin*
 When $N=1$ data is 2C
 $-2^n \leq A, B, R \leq 2^n-1$
 $(-2048) \quad (+2047)$

largest number is

$$\begin{array}{r} 4095 \\ + 4095 \\ \hline 8190 \end{array}$$

 $Cout=1$
 $R=4094$



7. Use the calculator to calculate radix 2 numbers. Data size is 12 bit. Apply the 2C convention for integers.

$$(36)_{10} = (100100)_2$$

36 18 9 4 2 1
 0 0 0 1 0 0
 0 0 0 1 0 0

$(000000100100)_2$

$$+2030 \equiv (\boxed{0}11111101110)_2$$

Sign bit

$$-2030 \equiv \boxed{1}00000010001 + 1$$

$$(\boxed{1}00000010010)_2$$

$$+1562 \equiv (\boxed{0}11000011010)_2$$

$$-1562 \equiv \boxed{1}00111100101 + 1$$

$$(\boxed{1}00111100110)_2$$

verify $2(2C(x)) = x \rightarrow$

$$\begin{array}{r} 011000011001 \\ + 1 \\ \hline 011000011010 \end{array}$$

$$(157)_{10} = (10011101)_2$$

$$(3571)_{10} = (11011110011)_2$$

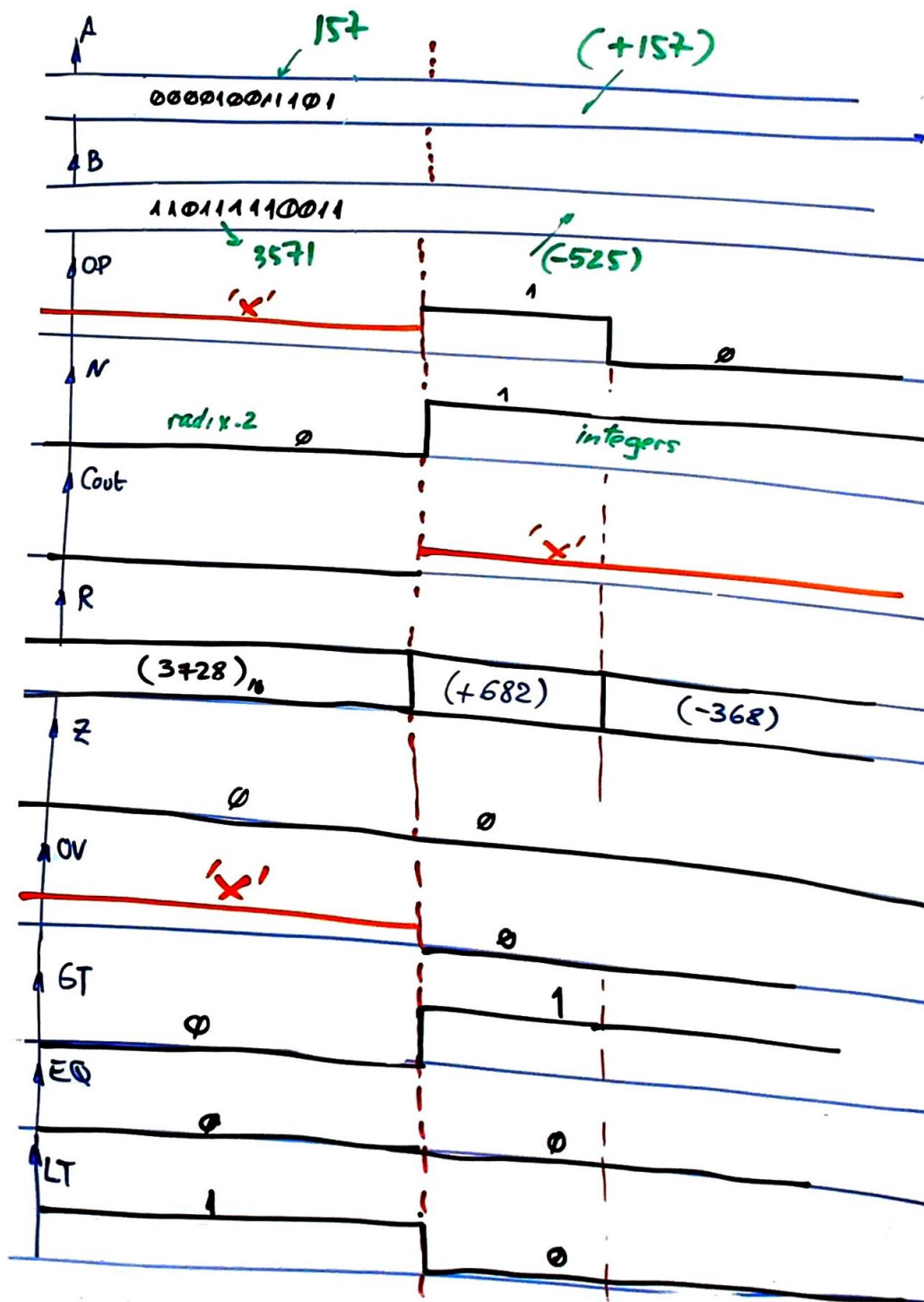
$(00010011101)_2$
 Twelve wires

8. Min_Pulse = 105 ns

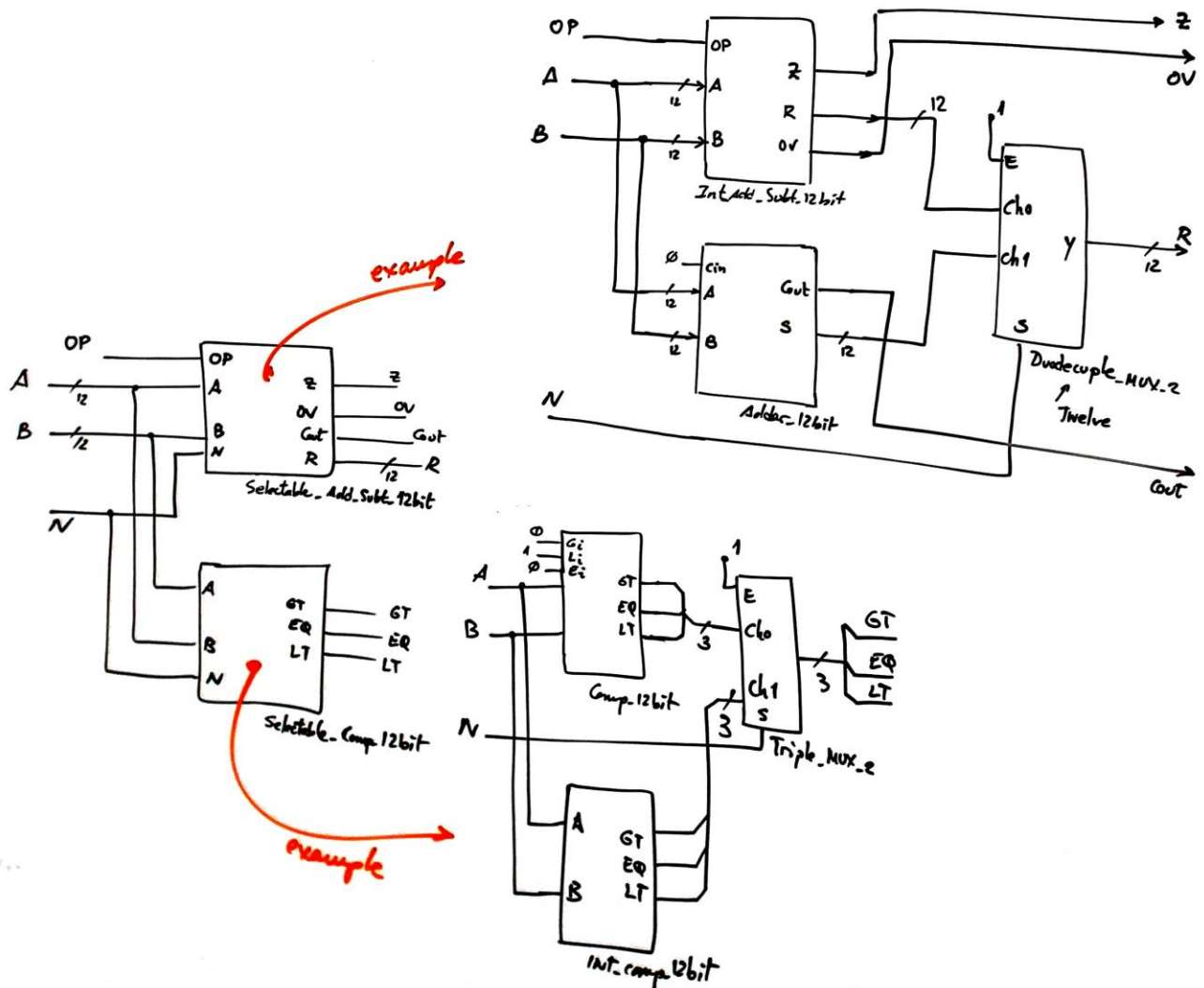
$$2^{12} \cdot 2^{12} \cdot 2^1 \cdot 2^1 = 2^{26} = 67108864 \text{ combinations}$$

Automating the test bench for generating all test vectors, it will take:

$$\text{run time} = 2^{26} \cdot \text{Min_Pulse} = 7.05 \text{ s}$$



9. Plan C2 allows top-down architecture organisation using simpler components. In a second phase, circuits can be optimised reducing the number of components and multiplexers.



10. Solved for 8-bits at P4: <https://digsys.upc.edu/csd/P04/P4.html>

11. Solved at this P3 tutorial: https://digsys.upc.edu/csd/P03/Comp_4bitC2/Comp_4bit.html

12. EQ is a bitwise XOR operation followed by a 12-input NOR gate.

First level of gates:

$$K_{11} = A_{11} \oplus B_{11}; K_{10} = A_{10} \oplus B_{10}; \dots K_0 = A_0 \oplus B_0$$

Then a second level $\rightarrow$ NOR

$$EQ = (K_{11} + K_{10} + \dots + K_1 + K_0)'$$

If the numbers are identical, all XOR outputs are 0, and so, $EQ = 1$

If any $A_i \neq B_i \rightarrow K_i = 1$, and thus $\rightarrow EQ = 0$

13. Solved for example in this P2 plan A tutorial on Adder_1bit:
https://digsys.upc.edu/csd/P03/Adder_1bit_A/Adder_1bit_A.html

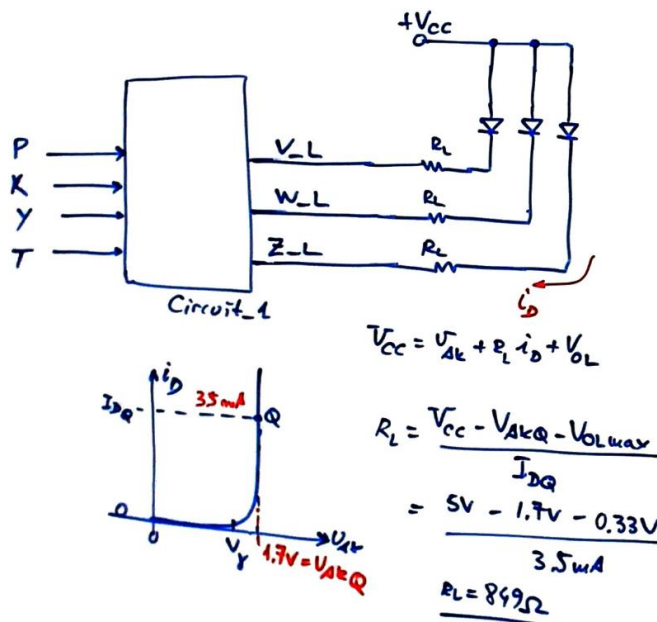
Ai	Bi	Ci	Co	So
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$$Co = f(Ai, Bi, Ci) = \prod M(0, 1, 2, 4)$$

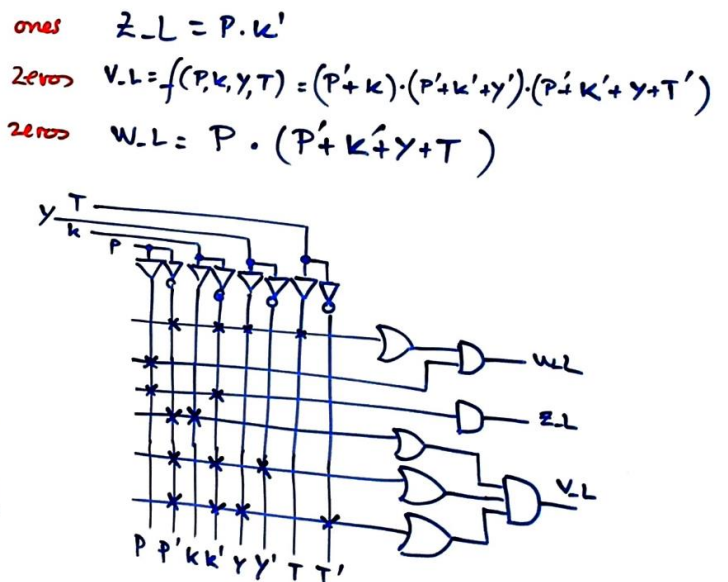
$$So = f(Ai, Bi, Ci) = \prod M(0, 3, 5, 6)$$

Problem 3

14.

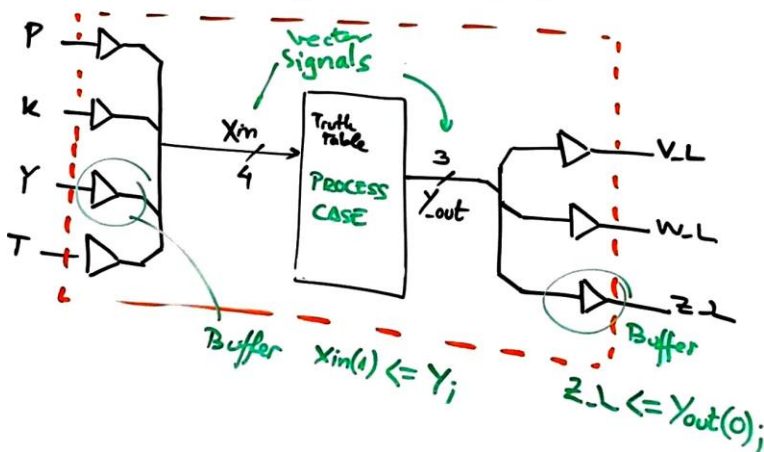


15.



16.

Expanding the 16 combinations, we can capture the truth table using buffers and signals and a single process



```

PROCESS (X_in)
CASE X_in IS
WHEN "0000" =>
Y_out <= "100";
WHEN "0001" =>
Y_out <= "100";
...
WHEN "1110" => Y_out <= "010";
WHEN others => Y_out <= "010";
END CASE;
END PROCESS;

```