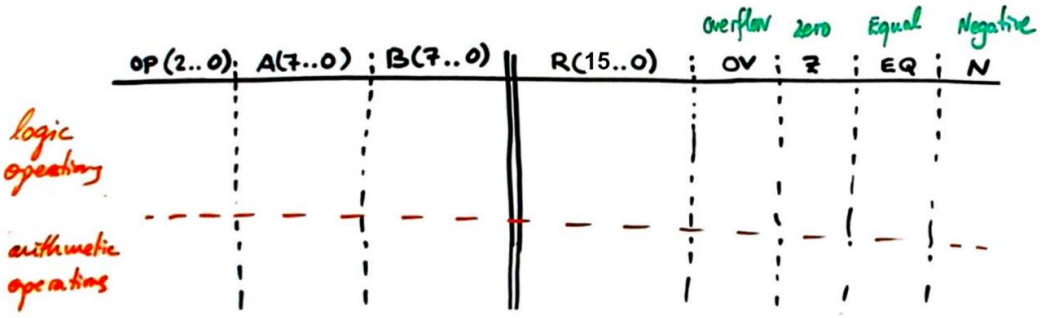
UPC. EETAC. Bachelor's degree. 2A. Digital Circuits and Systems (CSD). **Exam 1.** Grades available by 7th April.
Questions about exams and corrections: office time. **31st March**
(Problem 1) and (Problem 2) and [(Problem 3) or (Problem 4) or (Problem 5) or (Problem 6)]

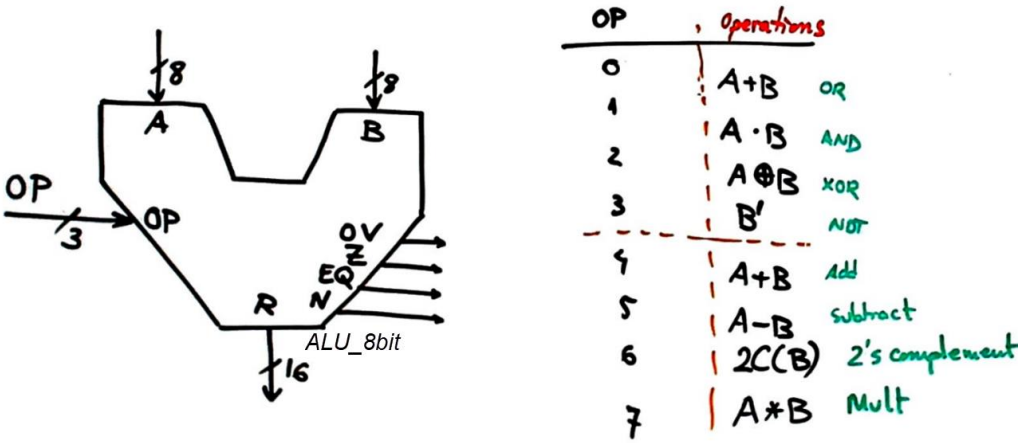
Problem 1 (4p)

For the ***ALU_8bit*** shown in Fig. 1a.

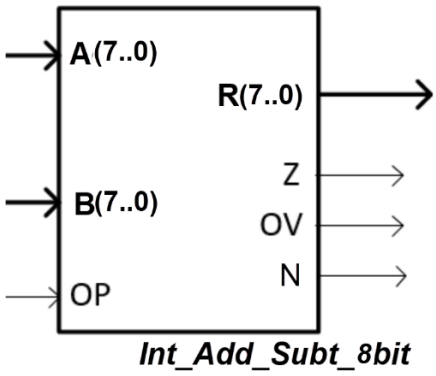
1. Indicate the range of the integer operands and results for the arithmetic operations in 2C. Complete the eight operations in binary for the following operands indicating as well the flag values when they care (check your results in decimal when necessary). Use a coloured square to indicate the position and value of the sign bit for arithmetic operations: **A** = "10111011"; **B** = "01001001"



2. Propose and explain the general architecture of the ALU designed internally using plan C2. Discuss using a timing diagram, which may be its maximum theoretical operational speed in Mops (millions of operations per second) if implemented using LS-TTL chips.
3. The ALU contains several chips and logic circuits; one of them is the chip ***Int_Add_Subt_8bit***, as shown in Fig. 1b, to perform additions and subtractions of 8-bit integer numbers in 2C. Draw a sketch plan C2 for this component. How many VHDL files will include this component?
4. Another component that we can find in the ALU is the ***Adder_1bit***. Design it in plan C2 using the method of multiplexers (MoM) with *MUX_2*. Apply some vectors to check that your circuit works as expected.



a)



b)

Fig. 1. a) 8-bit arithmetic and logic unit; b) one of *ALU_8bit* internal components used for performing the arithmetic operations 4, 5 and 6.

Problem 2 (3p)

1. Analyse the *Circuit_E* in Fig. 2 using method I to obtain its truth table **E** = *f*(**A**, **B**, **C**, **D**). Firstly, explain your plan and the concepts and procedures involved in the deduction.
2. What is maximum frequency of the generator f_{MAX} that we can use to drive an input? Calculate the power consumption when the circuit is running at such frequency. Calculate both parameters for implementations using (a) CMOS gates and (b) TTL_LS.
5. Invent the truth table using a plan A based on only NOR2 gates.

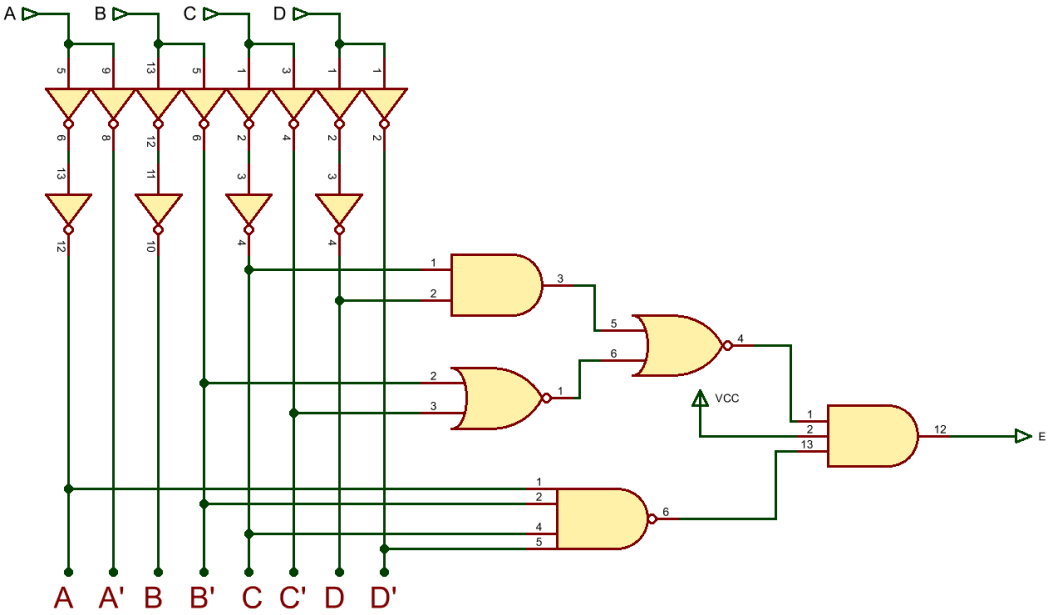


Fig. 2. Combinational circuit **E** = *f*(**A**, **B**, **C**, **D**).

Problem 3

The circuit in Fig. 3 is a 3-bit Gray decoder. (3p)

1. Complete the truth table. Obtain the outputs equations.
2. Connect LED active-high at each circuit output (V_{AKQ} = 1.9 V). Calculate the limiting resistors to drive each LED with 800 µA in the worst-case scenario using CMOS logic.
3. Describe the schematic or flowchart to be able to translate the truth table into VHDL using plan B.
4. Plan and solve the circuit using the method of decoders (MoD). Apply some vectors to check that your circuit works as expected.

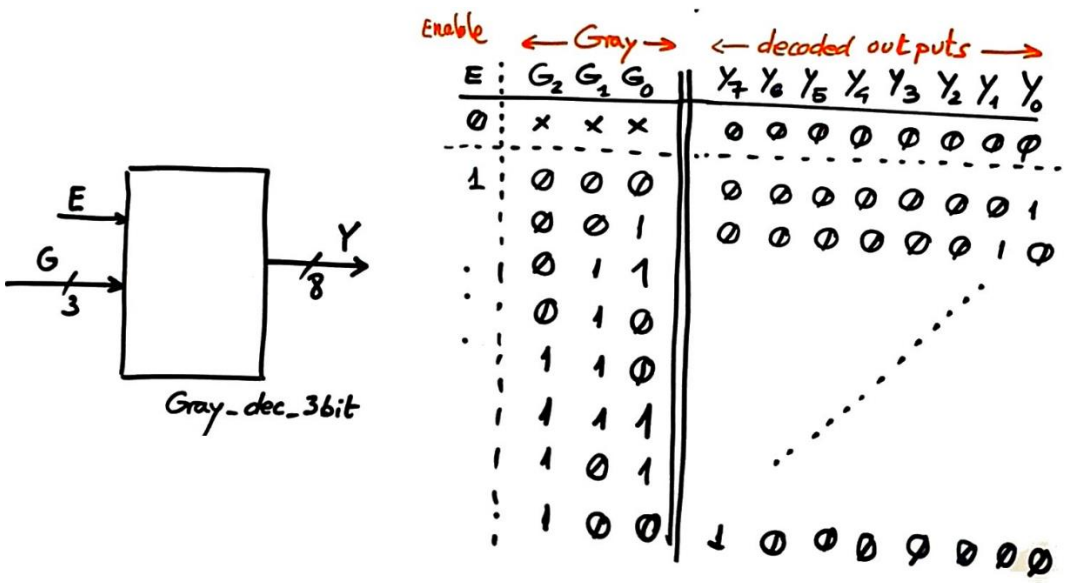
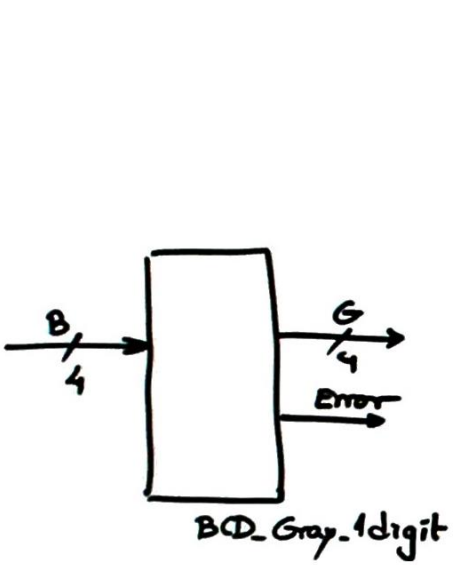


Fig. 3.

Problem 4 (3p)

The circuit in Fig. 4 is a combinational circuit to convert from 1-digit BCD to Gray code.

1. Complete the truth table. Obtain the canonical equations for G_2 and G_1 indicating the terms of no interest as *don't care* values.
2. If the circuit is solved completely using plan A, LS-TTL gates and simplified equations SoP or PoS from Minilog, calculate its propagation delay and maximum number of operations per second.
3. Plan and solve the circuit using the method of decoders (MoD). Apply some vectors to check that your circuit works as expected.
4. Invent a *Dec_4_16* using only *Dec_2_4* and logic gates if necessary.

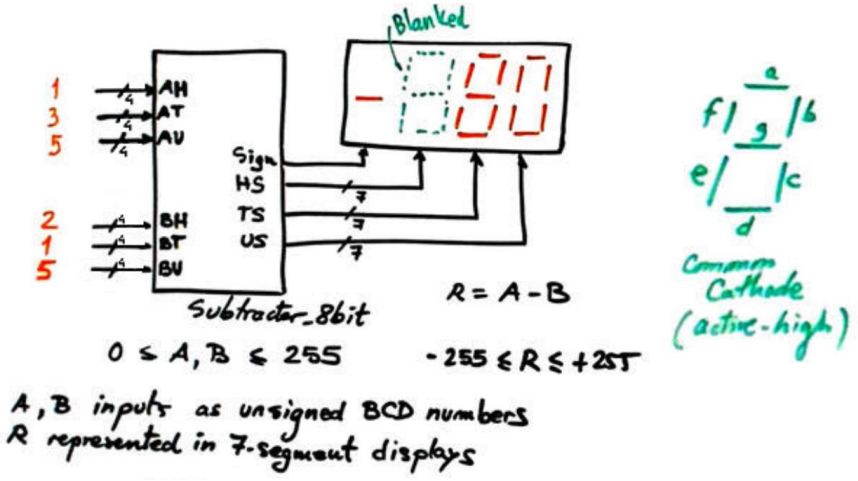


BCD				Gray				
B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0	Error
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	1	0
0	0	1	1	0	0	1	0	0
⋮				⋮				⋮
1	0	0	1					0
1	0	1	0	X	X	X	X	1
⋮				⋮				⋮

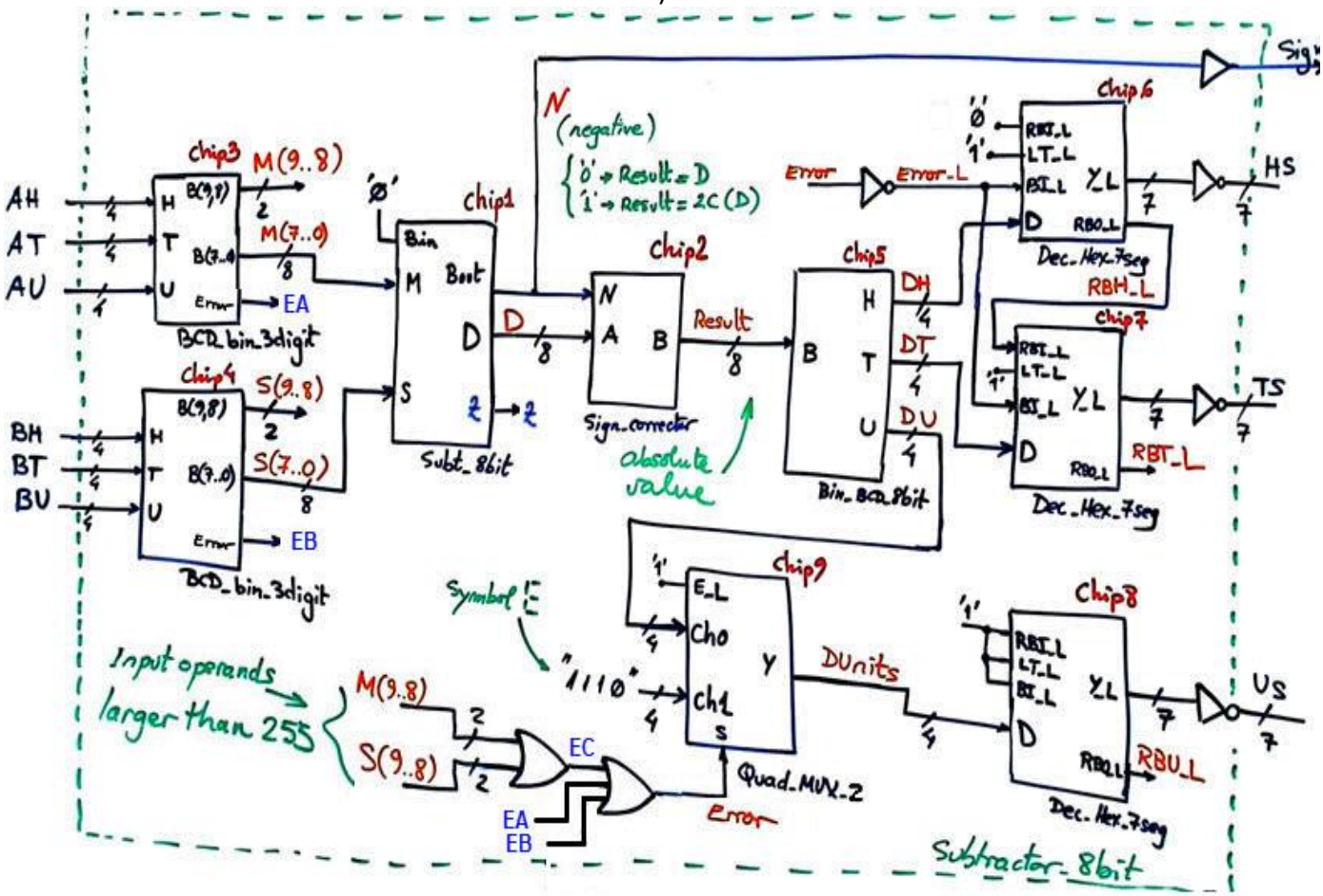
Fig. 4.

Problem 5 (3p)

We aim to design the subtractor **R** = **A** – **B** circuit in Fig. 5a capable of using 3-digit BCD operands and representing output results in 7-segment displays. Its proposed internal plan C2 structure is represented in Fig. 5b where we can see a simple *Subt_8bit* (Chip1) as the arithmetic circuit for radix-2 numbers.



a)



b)

Fig. 5. 8-bit subtractor and its proposed internal architecture.

1. Generate a timing diagram representing these operations: 135 – 215; 215 – 1B5; 155 – 32; 976 – 155.
2. If we can automate a VHDL test-bench, and all the input vector signals last for *Min_Pulse* = 3.4 μs, how long will it take to check all the truth table?
3. Deduce all the outputs and internal signals while explaining the functionality of each component: Sign, HS, M, S, D, etc. for the following operation: 976 – 155.
4. Explain what is the idea behind the chain RBO_L → RBI_L implemented for several *Dec_Hex_7seg*.

Problem 6 (3p)

The decoder from hexadecimal to 7-segment *Dec_Hex_7seg* represented in Fig. 6 works as indicated in the truth table.

1. Describe a flowchart to be able to translate the truth table in VHDL using plan B.
2. Complete the circuit's truth table. How many maxterms contains **a_L**? How many logic gates will the circuit contain if solved using plan A and simpler equations SoP or PoS from Minilog or by truth table inspection? Which is power consumption of the circuit working at the maximum theoretical number of decoding operation per second if LS-TTL gates are used? Imagine all the circuit gates switching.
3. Calculate the limiting resistor R1 to drive the LED segments at V_{AKQ} = 2.1 V, I_{DQ} = 1.2 mA.

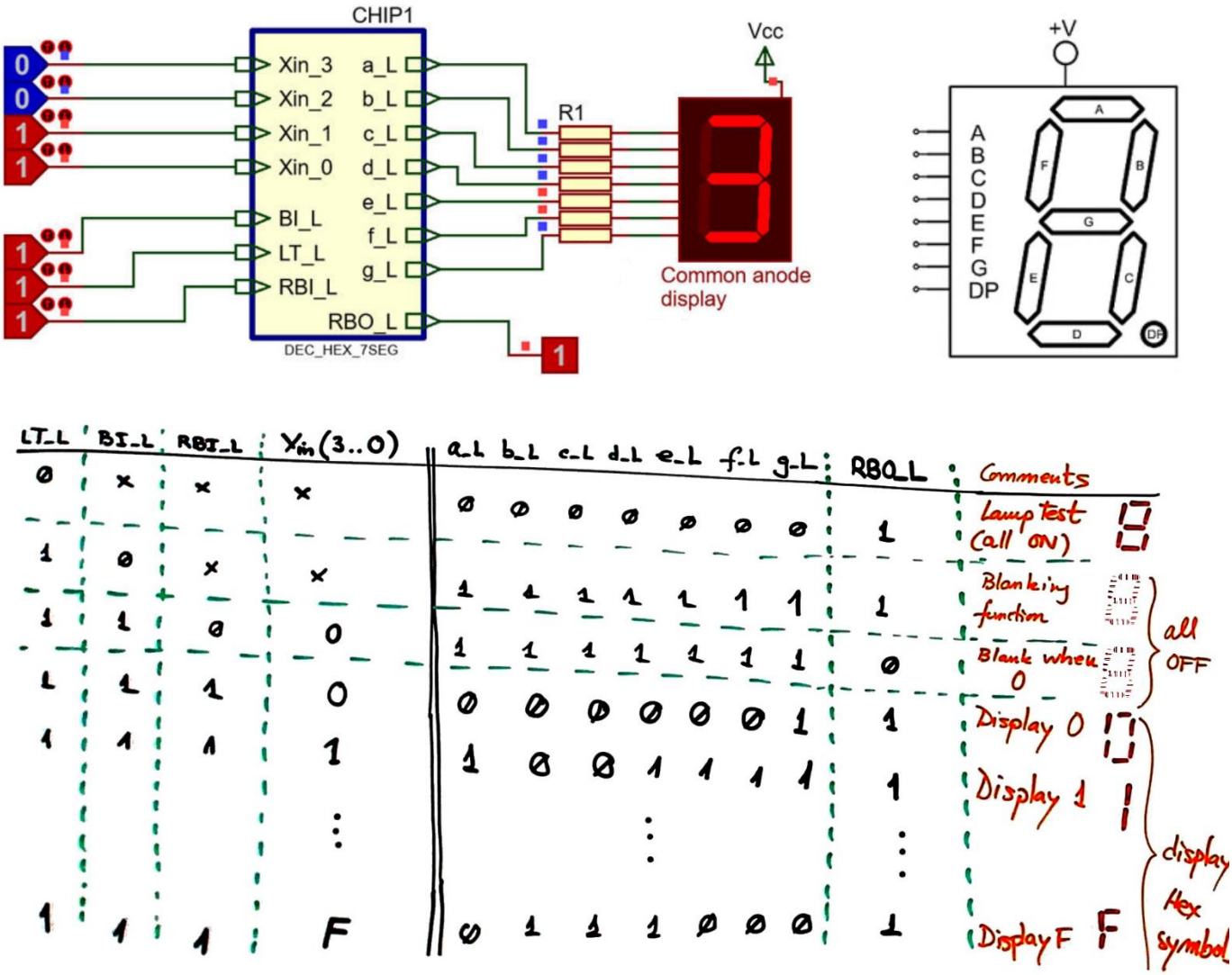
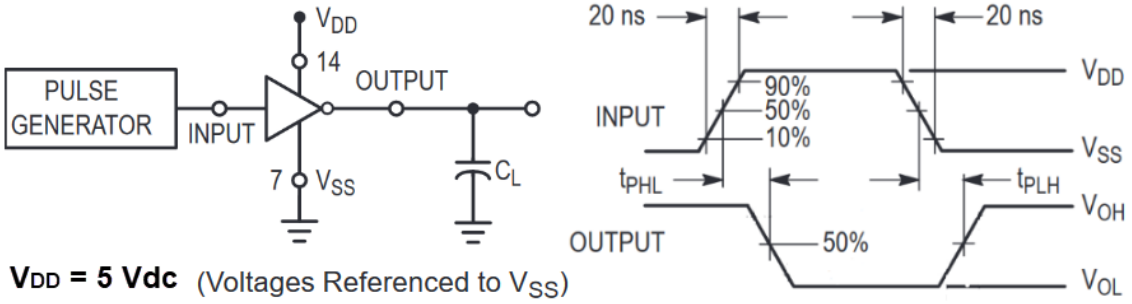


Fig. 6. Idea of the decoder *Dec_Hex_7seg* truth table used for driving active-low LED segments.

Annex. Fig. 7 shows the electrical characteristics of a single logic gate in classic CMOS

$$P_S + P_{dyn} = I_{DDQ} \cdot V_{DD} + V_{DD}^2 \cdot C_L \cdot f$$

MC14069UB 	Symbol	25°C			Unit
		Min	Typ	Max	
Output Voltage V_{in} = V_{DD} "0" Level	V_{OL}	—	0	0.05	Vdc
V_{in} = 0 "1" Level	V_{OH}	4.95	5.0	—	Vdc
Input Voltage "0" Level (V_O = 4.5 Vdc)	V_{IL}	—	2.25	1.0	Vdc
"1" Level (V_O = 0.5 Vdc)	V_{IH}	4.0	2.75	—	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	– 2.4	– 4.2	—	mAdc
(V_{OH} = 4.6 Vdc)		– 0.51	– 0.88	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	0.51	0.88	—	mAdc
Input Current	I_{in}	—	±0.00001	± 0.1	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	5.0	7.5	pF
Quiescent Current (Per Gate)	I_{DD}	—	0.084	42	nAdc
Total Supply Current (C_L = 50 pF) (Dynamic plus Quiescent(Per Gate)	I_T	I_T = (0.3 µA/kHz) f + I_{DD}			µAdc
Propagation Delay Times (C_L = 50 pF) t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 20 ns	t_{PLH}, t_{PHL}	—	65	125	ns



V_{DD} = 5 Vdc (Voltages Referenced to V_{SS})

Fig. 7. Characteristics of a logic gate in CMOS technology

Annex. Fig. 8 shows the characteristics of a single logic gate in LS-TTL technology.

$$P_S + P_{dyn} = I_{DDQ} \cdot V_{DD} + V_{DD}^2 \cdot C_L \cdot f$$

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			–0.4	mA
I_{OL}	LOW Level Output Current			8	mA

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = –18 mA			–1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			–0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	–20		–100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		1.2	2.4	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		3.6	6.6	mA

Symbol	Parameter C_L = 50 pF	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	4	15	ns

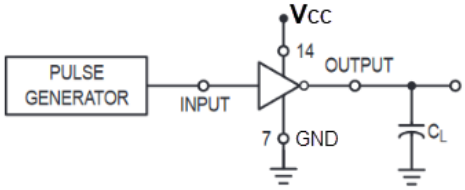

Fig. 8. Characteristics of a logic gate in LS-TTL technology

NOTE for all problems and questions: draw circuits, sketches or diagrams, explain as clearly as possible what you do and how you are inventing circuits or processing calculations as you did when you wrote your project reports. Justify your results.