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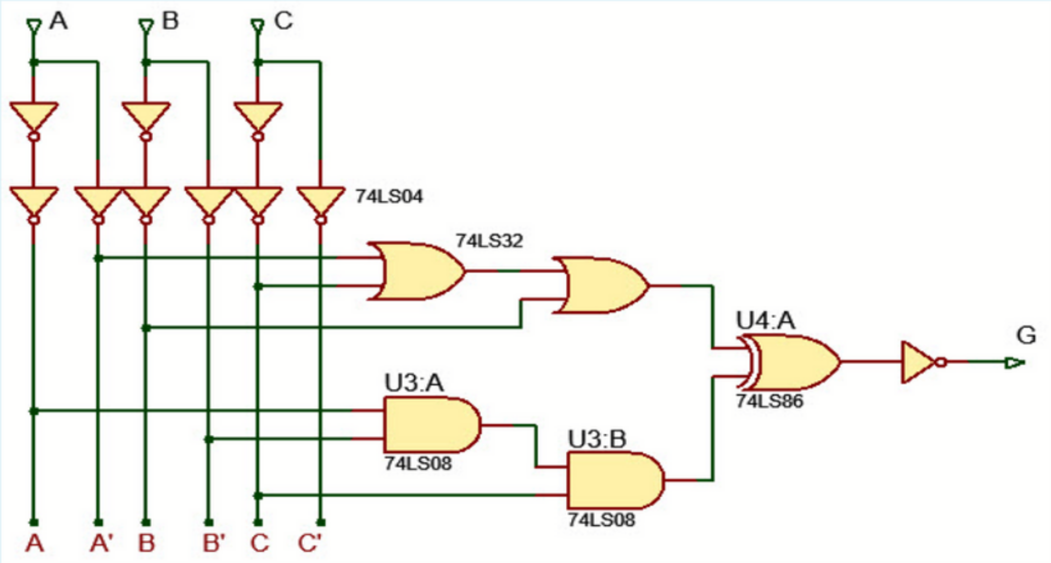
Sample questions for projects P1- P2 - P3 - P4

Analyse the circuit in the picture and deduce the output G = *f* (A, B, C).



Select one:

- ○ a. $G = (A' + B + C) \oplus (AB'C)$
- ◉ b. $G = ((A' + B + C) \cdot (A' + B + C') + (A' + B + C)' \cdot (AB'C))'$
- ○ c. $G = ((A + B' + C') \cdot (AB'C)' + (A' + B' + C)' \cdot (AB'C))'$

For a boolean function of *n* variables x_1, ..., x_n, a sum term in which each of the *n* variables appears **once** (in either its complemented or uncomplemented form) is called a ***maxterm***.

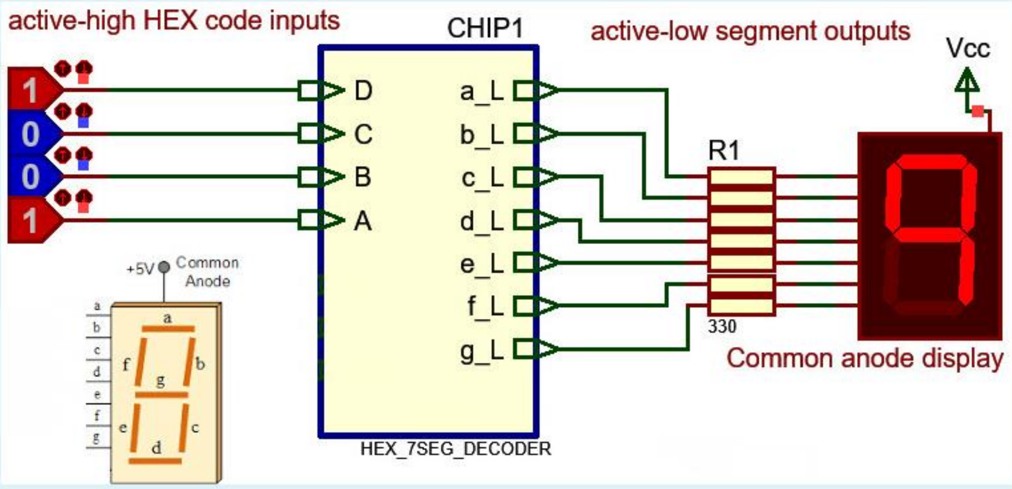
A single maxterm *n* gives a '0' value for just one combination of the input variables. Thus, it is possible to write the truth table of a logical function as a product of maxterms.

Select one:

Answers

- ◉ True
- ○ False

This circuit is a hexadecimal to seven-segment decoder which has active-low outputs. The number '9' is represented. Which is the value of the output vector $[a\_L, b\_L, c\_L, \ldots . g\_L]$?



Select one:

- a. [1 1 1 0 0 1 1]
- b. [1 1 1 0 0 1 0]
- c. [0 0 0 1 1 0 1]
- d. [0 0 0 1 1 0 0]

The picture shows the truth table resulting from the WolphamAlpha numerical engine when ordered to obtain it. The function is described as: $P = f(D1, D0, A, B)$ Thus, find the sum of minterms.

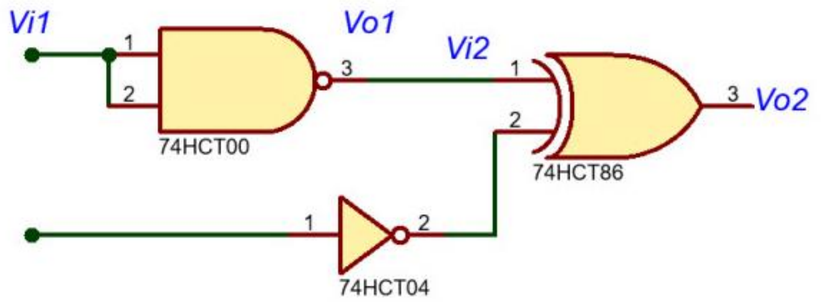
Truth table:

A	B	D0	D1	**P**
T	T	T	T	T
T	T	T	F	T
T	T	F	T	F
T	T	F	F	F
T	F	T	T	F
T	F	T	F	T
T	F	F	T	T
T	F	F	F	T
F	T	T	T	F
F	T	T	F	F
F	T	F	T	T
F	T	F	F	T
F	F	T	T	T
F	F	T	F	F
F	F	F	T	F
F	F	F	F	T

Select one:

- a. $P = f(D1, D0, A, B) = \sum m(0, 1, 2, 6, 7, 9, 10, 12, 15)$
- b. $P = f(D1, D0, A, B) = \sum M(3, 4, 5, 8, 11, 13, 14)$
- c. $P = f(D1, D0, A, B) = \sum m(0, 1, 5, 6, 7, 10, 11, 12, 15)$

This circuit is build using gates of the HCT (High Speed CMOS) technology that has the characteristics given below. Which statement is false?



DC Electrical Specification *Vcc = 4.5 V*

PARAMETER	SYMBOL	25°C			UNITS
		MIN	TYP	MAX	
HC TYPES					
High Level Input Voltage	V_{IH}	3.15	-	-	V
Low Level Input Voltage	V_{IL}	-	-	1.35	V
High Level Output Voltage	V_{OH}	4.4	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.1	V

Select one:

○ a. $V_{IL\ max}$ is the maximum voltage that can understand V_{i2} as a logic '0'

◉ b. In good operation conditions, when generating a low '0', V_{O1} can be higher that $V_{OL\ max}$ = 0.1 V

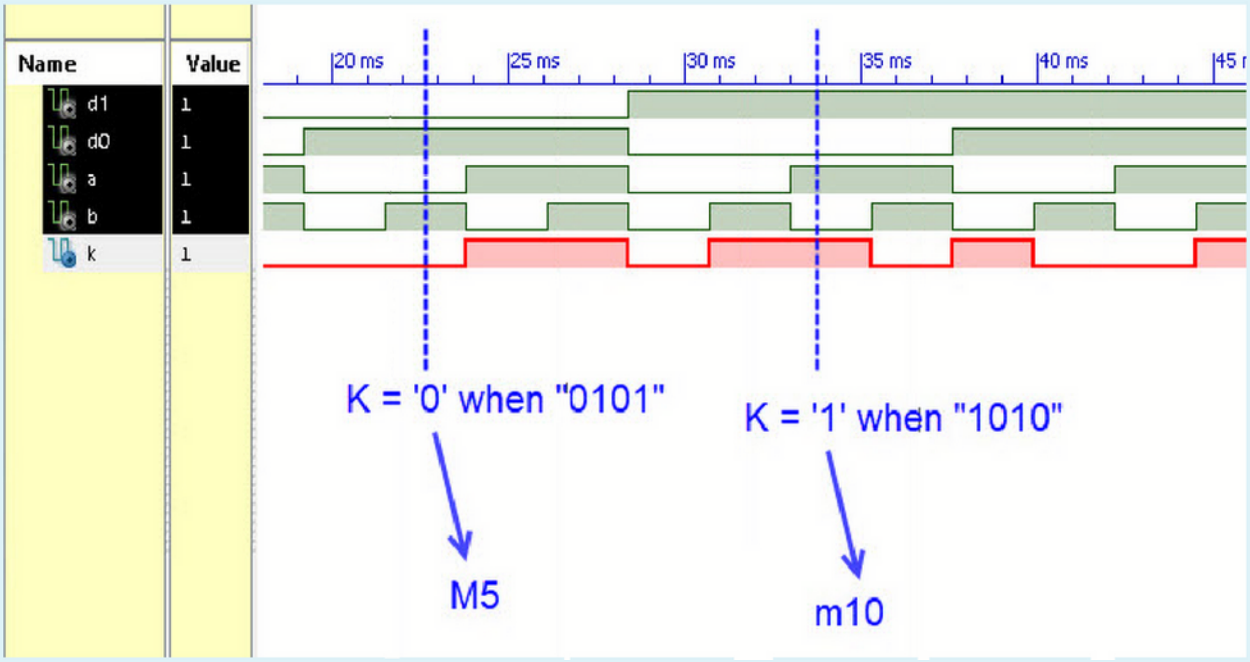
○ c. If V_{O1} is below the the $V_{OH\ min}$ = 4.4 V the next gate input voltage V_{i2} may not understand it as a valid '1' .

○ d. If the NAND gate is operating correctly, when generating an output level '1', V_{O1} is always above the the threshold $V_{OH\ min}$ = 4.4 V

Running the EDA VHDL simulator and examining the output timing diagram we can determine the truth table of a given circuit. For instance, in the capture below, we measure that:

K = f(D1, D0, A, B) = K(1100) = **0** → M_{12}

K(1001) = **1** → m_9

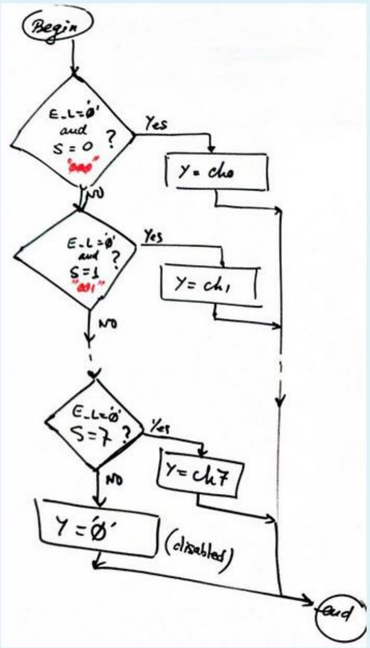


Select one:

Answers

- ○ True
- ◉ False

We plan a VHDL behavioural description of a **MUX_8** as shown in the flow chart sketch below. We have found up to three possible circuits to **copy & adapt** from the *digsys* web belonging to MUX_4 projects. Which is preferred one?



Select one:

○ a.

```
SIGNAL  X_in    : STD_LOGIC_VECTOR (5 downto 0);
BEGIN

    Y <= '0'when std_match(X_in,"00---0") and E_L = '0' else
         '1'when std_match(X_in,"00---1") and E_L = '0' else
         '0'when std_match(X_in,"01--0-") and E_L = '0' else
         '1'when std_match(X_in,"01--1-") and E_L = '0' else
         '0'when std_match(X_in,"10-0--") and E_L = '0' else
         '1'when std_match(X_in,"10-1--") and E_L = '0' else
         '0'when std_match(X_in,"110---") and E_L = '0' else
         '1'when std_match(X_in,"111---") and E_L = '0' else
         '0';


-- Extra logic (simple buffers in this case)

X_in(5) <= S(1);
X_in(4) <= S(0);
X_in(3) <= Ch3;
X_in(2) <= Ch2;
X_in(1) <= Ch1;
X_in(0) <= Ch0;
```

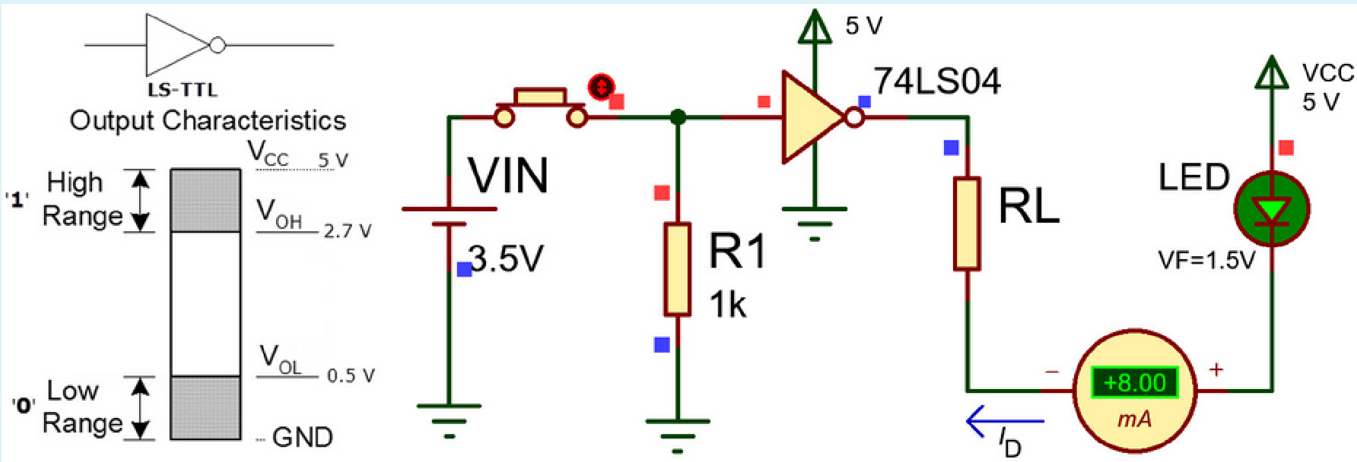
◉ b.

```
architecture truth_table of MUX_4 is
begin
y   <=   Ch0 when (s ="00" and E_L = '0') else
         Ch1 when (s ="01" and E_L = '0') else
         Ch2 when (s ="10" and E_L = '0') else
         Ch3 when (s ="11" and E_L = '0') else '0';

end truth_table;
```

○ c.

```
BEGIN

    PROCESS ( E_L, S, Ch3,Ch2,Ch1,Ch0)
        BEGIN
            IF E_L = '1' THEN
                Y <= '0';    -- disable
            ELSE
                IF S = "00" THEN y <= Ch0;
                ELSIF S = "01" THEN y <= Ch1;
                ELSIF S = "10" THEN y <= Ch2;
                ELSE y <= Ch3;
                END IF ;
            END IF ;
    END PROCESS;
END truth_table;
```

Which is the value of the limiting resistor R_L that bias the LED with $I_D = 8mA$ in the worst case scenario?



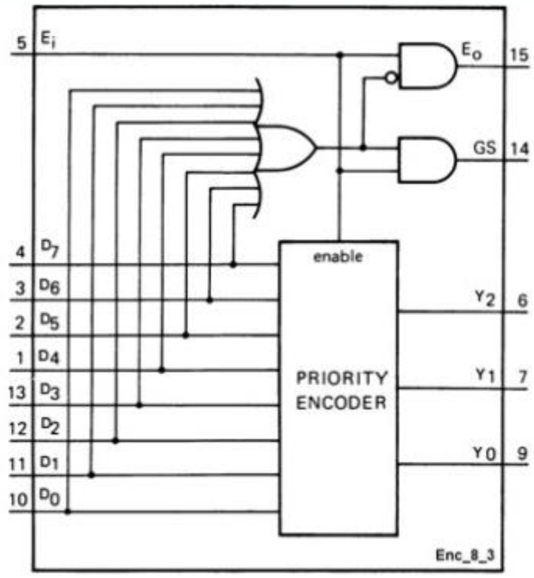
Select one:

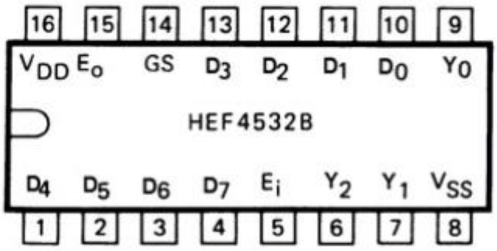
◉ a. $R_L = 375\ \Omega$

○ b. $R_L = 150\ \Omega$

○ c. $R_L = 437.5\ \Omega$

This is a HEF4532B, a commercial encoder 8 to 3 with priority high. How many minterms have the outputs GS and Y0?



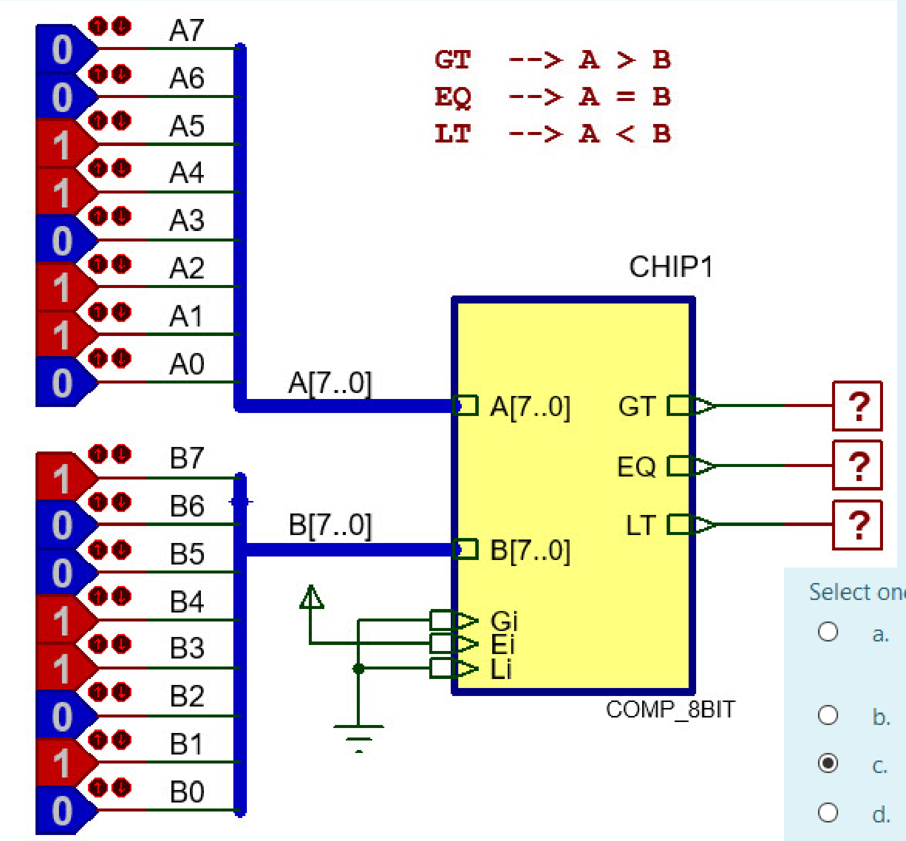


				inputs							outputs		
Ei	D7	D6	D5	D4	D3	D2	D1	D0	GS	Y2	Y1	Y0	Eo
0	x	x	x	x	x	x	x	x	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	1	1	0	0	0	0
1	0	0	0	0	0	0	1	x	1	0	0	1	0
1	0	0	0	0	0	1	x	x	1	0	1	0	0
1	0	0	0	0	1	x	x	x	1	0	1	1	0
1	0	0	0	1	x	x	x	x	1	1	0	0	0
1	0	0	1	x	x	x	x	x	1	1	0	1	0
1	0	1	x	x	x	x	x	x	1	1	1	0	0
1	1	x	x	x	x	x	x	x	1	1	1	1	0

Select one:

- ○ a.
  GS has 8 minterms and **Y0** has 6 minterms.
- ◉ b.
  GS has 255 minterms and **Y0** has 170 minterms.
- ○ c.
  GS has 2 minterms and **Y0** has 6 minterms.

The circuit in the picture is a *Comp_8bit*, a comparator of radix-2 binary numbers. Which is the output of the circuit when driven by these input vectors?



Select one:

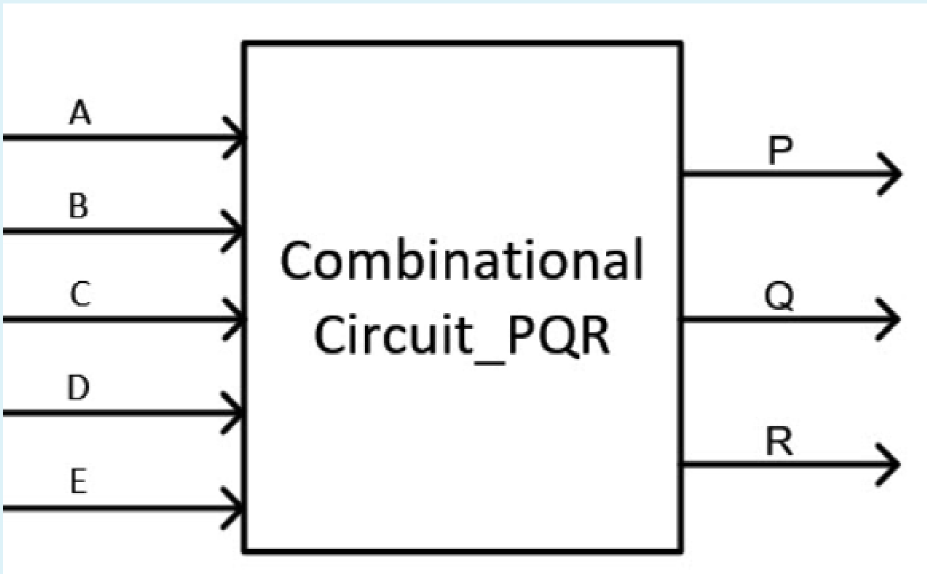
a. $\mathbf{GT} = '1';\ \mathbf{EQ} = '0';\ \mathbf{LT} = '0'$

b. $\mathbf{GT} = '1';\ \mathbf{EQ} = '1';\ \mathbf{LT} = '0'$

c. $\mathbf{GT} = '0';\ \mathbf{EQ} = '0';\ \mathbf{LT} = '1'$

d. $\mathbf{GT} = '0';\ \mathbf{EQ} = '1';\ \mathbf{LT} = '0'$

The *Circuit_PQR* in the picture is planned on the method of decoders, and the decoder is build internally chaining 4 components *DEC_3_8*. How many VHDL files will contain this hierarchical structural project?



Select one:

a. 6 VHDL files

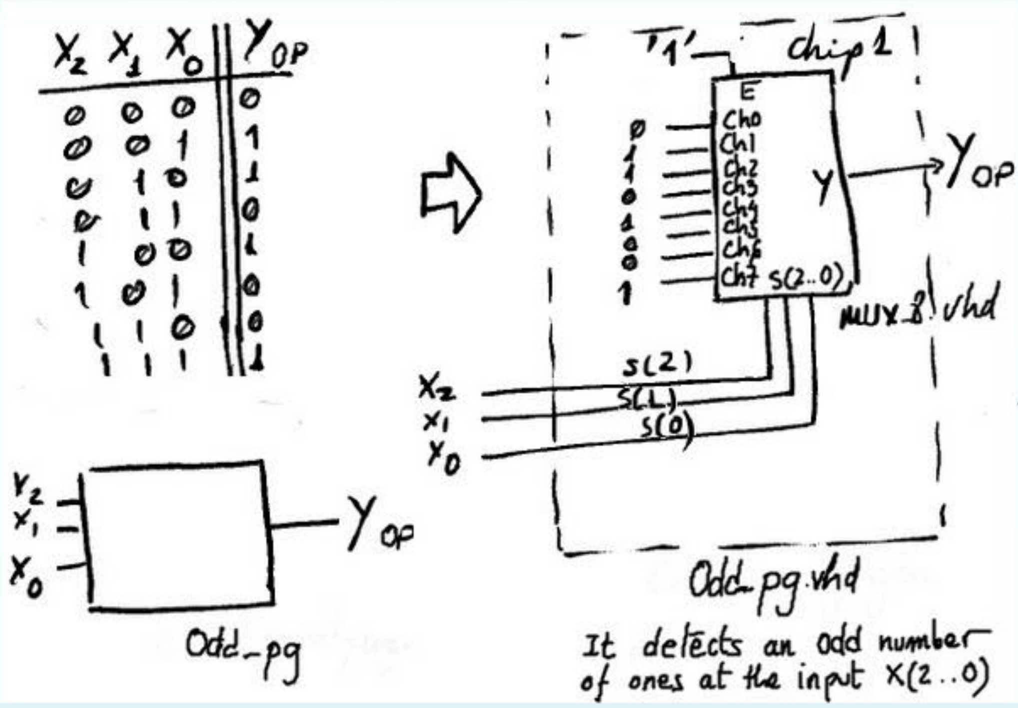
b. 4 VHDL files

c. 1 VHDL files

d. 3 VHDL files

The circuit below is a 3-bit odd-parity generator solved using the method of multiplexers and a MUX_8. Furthermore, the MUX_8 component is build internally using MUX_2. The resulting Y_{OP} = f(X2, X1, X0) is faster (less propagation delay) than the circuit produced using maxterms

$$Y_{OP} = f(X_2, X_1, X_0) = \prod\{0, 3, 5, 6\}$$

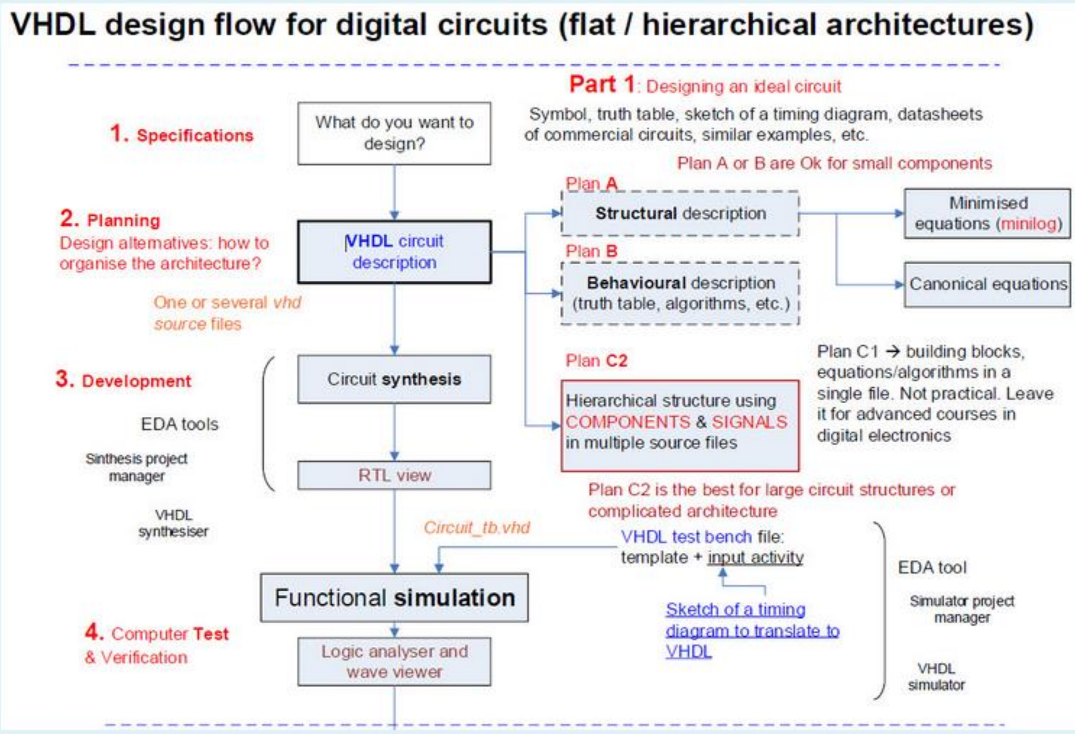


Select one:

Answers

- ○ True
- ◉ False

The step number 4 in this design flow, the functional simulation, allows you to measure gate delays, propagation times and the worst case scenario to deduce the maximum frequency of operation of the designed circuit.

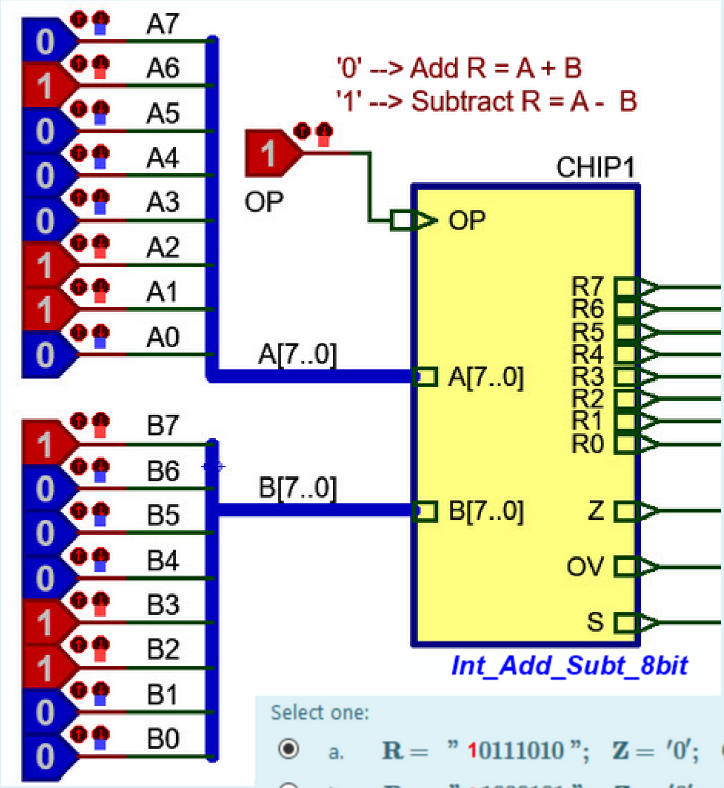


Select one:

Answers

- ○ True
- ◉ False

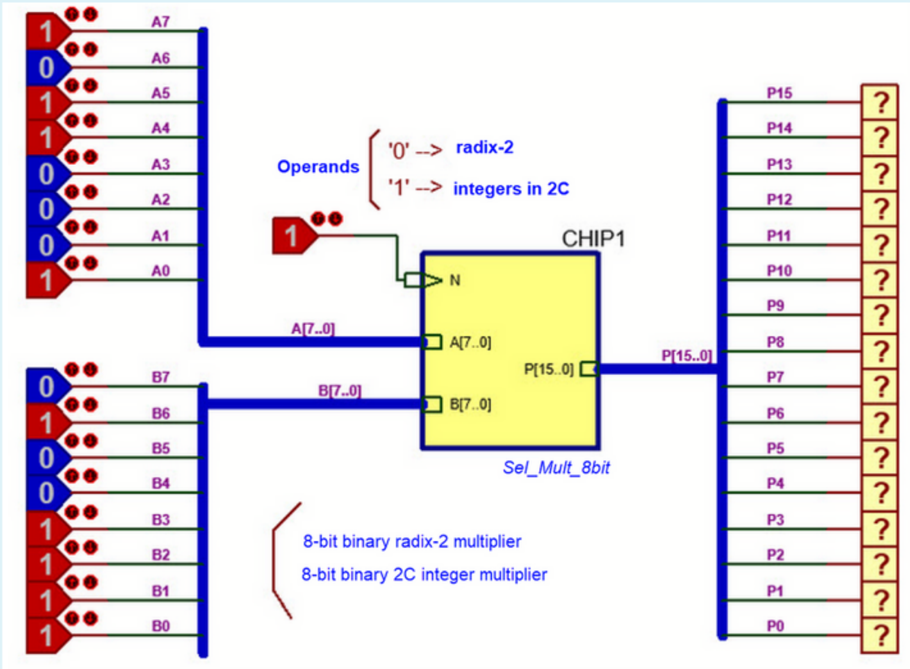
Which is the output of the circuit ?



Select one:

- a. R = " 10111010 "; Z = '0'; OV = '1'; S = '1'
- b. R = " 01000101 "; Z = '0'; OV = '0'; S = '0'
- c. R = " 10111010 "; Z = '0'; OV = '0'; S = '1'

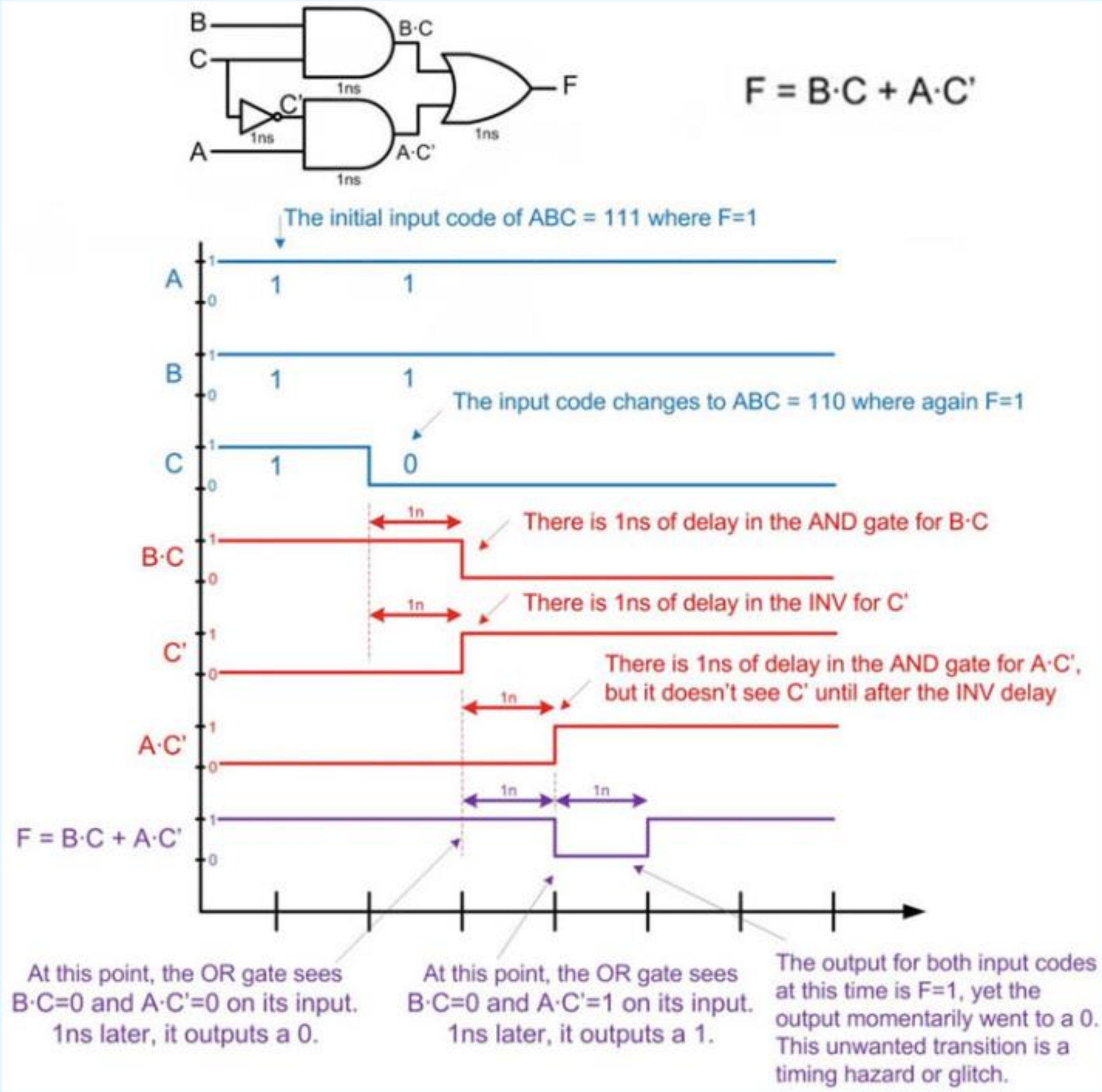
The circuit in the picture is a *Sel_Mult_8bit* , a binary multiplier that has a control input **N** to operate with radix 2 data when **N** = 0, and with two's complement data when **N** = 1. Which is the output of the circuit when driven by these input vectors?



Select one:

- a. $P(15..0) =$" 1110 0111 1001 1111 "
- b. $P(15..0) =$" 1001 1111 0111 1111 "
- c. $P(15..0) =$" 0011 0110 1001 1111 "

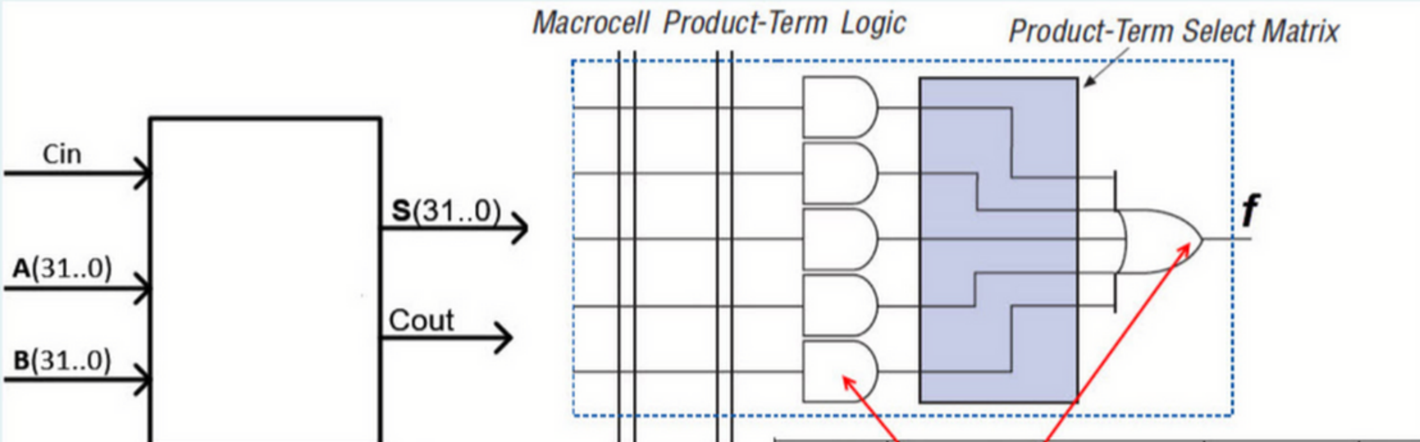
Timing hazards or glitches refer to unwanted transitions on the output of a combinational logic circuit. These are most commonly due to different delay paths through the gates in the circuit. In real circuitry there is always a finite propagation delay through each gate. Consider the circuit analysed below where a timing diagram shows signal transitions and hand-made annotations.



Select one:

- ○ a. Using VHDL test benches we can measure the circuit's delay such as here (3 ns) using the functional simulation EDA tool.
- ◉ b. Using VHDL test benches we can measure the circuit's delay such as here (3 ns) using the gate-level simulation EDA tool.
- ○ c. Using VHDL test benches we can measure the circuit's delay such as here (2 ns) using the gate-level simulation EDA tool.
- ○ d. Using VHDL test benches we can measure the circuit's delay such as here (2 ns) using the functional simulation EDA tool.

The *Adder_32bit* entity in the picture is based on the ripple-carry technique of 32 *Adder_1bit* cells, which internally are structured using 3-levels-of-logic gates as shown in the simplified macrocell. The entity is implemented in an Intel-Altera CPLD MAX7128S chip showing the technology characteristics in the table. Calculate the circuit's propagation delay and its maximum speed of operation.



Symbol	Parameter	Speed Grade		Unit
		Min	Max	
t_{Pg}	Logic gate delay		3.0	ns

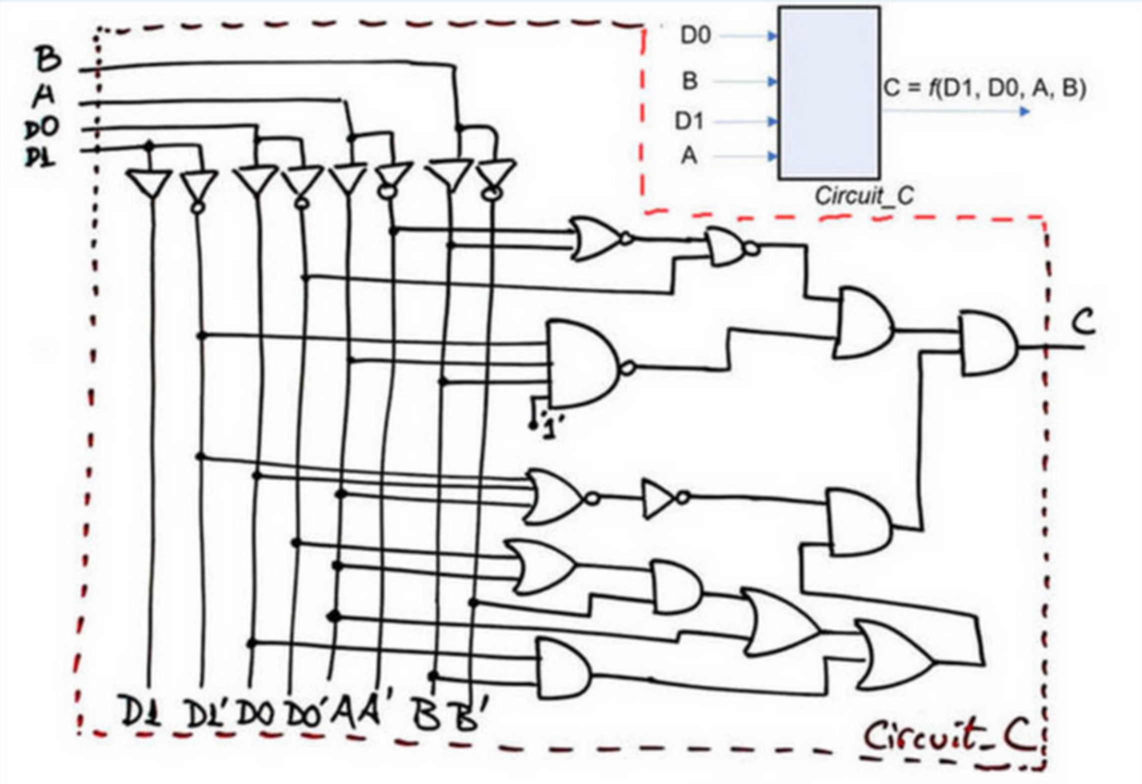
EPM7128S Internal Timing Parameters

Select one:

- ○ a. Propagation time t_P = 3 ns; speed = 333 millions of operations per second
- ◉ b. Propagation time t_P = 288 ns; speed = 3.4 millions of operation per second
- ○ c. Propagation time t_P = 96 ns; speed = 10.4 millions of operations per second

The *Circuit_C* in the picture is built using 74LS logic gates. Which is its propagation delay t_P and its theoretical speed (or maximum operating frequency or number of operations per second or the number of times per second that it is capable of calculating the truth table)?

If we mount the circuit in the laboratory and apply a signal generator to one of the inputs, which is the maximum frequency of the generator f_{max}?



Switching Characteristics 74LS Gates

at $V_{CC} = 5V$ and $T_A = 25°C$

Symbol	Parameter	$R_L = 2\ k\Omega$		Units
		$C_L = 15\ pF$		
		Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	10	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	ns

Select one:

- a. Propagation time t_P = 21 ns ; speed = 47.6 millions of operations per second; generator frequency = f_{max} = 23.8 MHz
- b. Propagation time t_P = 3 ns ; speed = 166 millions of operations per second; generator frequency = f_{max} = 166 MHz
- c. Propagation time t_P = 70 ns ; speed = 14.2 millions of operations per second; generator frequency = f_{max} = 7.1 MHz
- d. Propagation time t_P = 70 ns ; speed = 14.2 millions of operations per second; generator frequency = f_{max} = 14.2 MHz