CSD laboratory P_Ch3: µC-based programmable timer

I. Specifications

The aim of this project is to invent a digital programmable timer.
Features:

- Programmable 16-bit pulse count (**PC**)
- 1 kHz external **CLK** reference (T_{CLK} = 1ms) (or equivalent internal TMR0 time base in design phase #3)
- End of timing period pulse (**ETP**) flag (width = 50·T_{CLK}, 50 ms)
- Active-high interrupt-driven **TRG** pulse
- Asynchronous reset
- Timed output signal **Timer_out** = PC · T_{CLK} (maximum timing period = 65535 ms)
- MICROCHIP PIC18F4520 microcontroller chip
- Dedicated processor architecture for adapting concepts and P_Ch2 planning
- LCD display for representing ASCII messages indicating timer operation

Fig. 1 shows the chip symbol at design phase #2 and an example of typical waveforms.

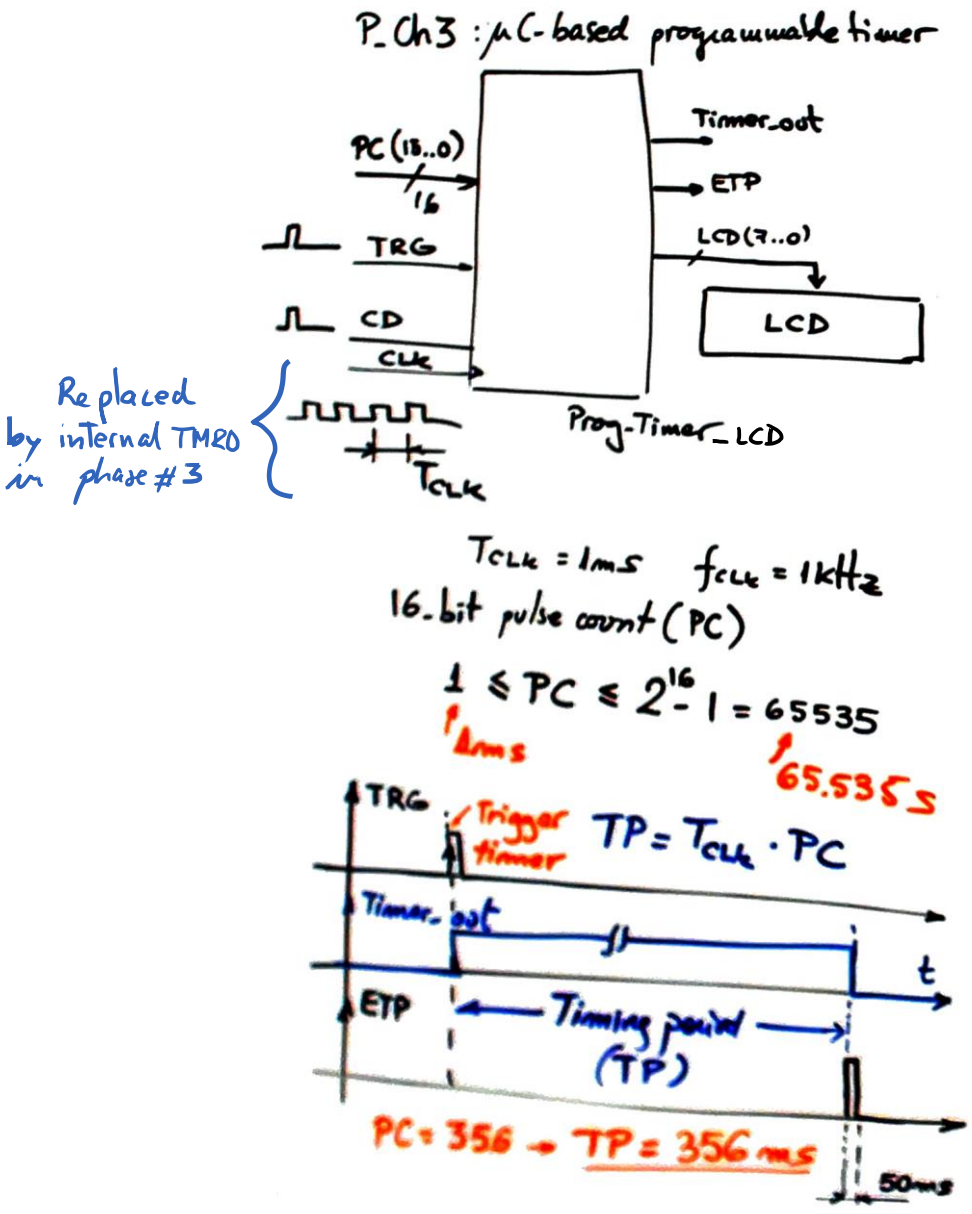

Fig. 1 Symbol and typical waveforms in design phase #2. A **TRG** pulse, for instance clicking a button, triggers the timing period. Once the timing period (**TP**) ends, a single pulse of 50·T_{CLK} duration is generated to indicate that the device is idle and can be used again for programing any other timing interval. This device is non-retriggerable, meaning that other trigger pulses are ignored while the device is on duty.

One of the goals of the project is to compare features and performance with P_Ch2.

Extra features may be added optionally introducing new design phases once this basic project is complete and operates correctly:

- Retriggerable switch to be able to generate arbitrary large timing periods.
- TMR2 instead of TMR0 to obtain higher precision.
- Alarm sound to indicate end of timing period.
- Serial (RS232) or keypad pulse count programing, etc.

II. Planning

To make it simple and reasonable in the given time constraints and to be able to embed its design within CSD course timeline, we propose adapting to uC the architecture designed in P_Ch2. Fig. 2 shows the proposed hardware circuit for design phase #2. Additional resources, diagrams, sections of C code and support will be given to speed up the design.

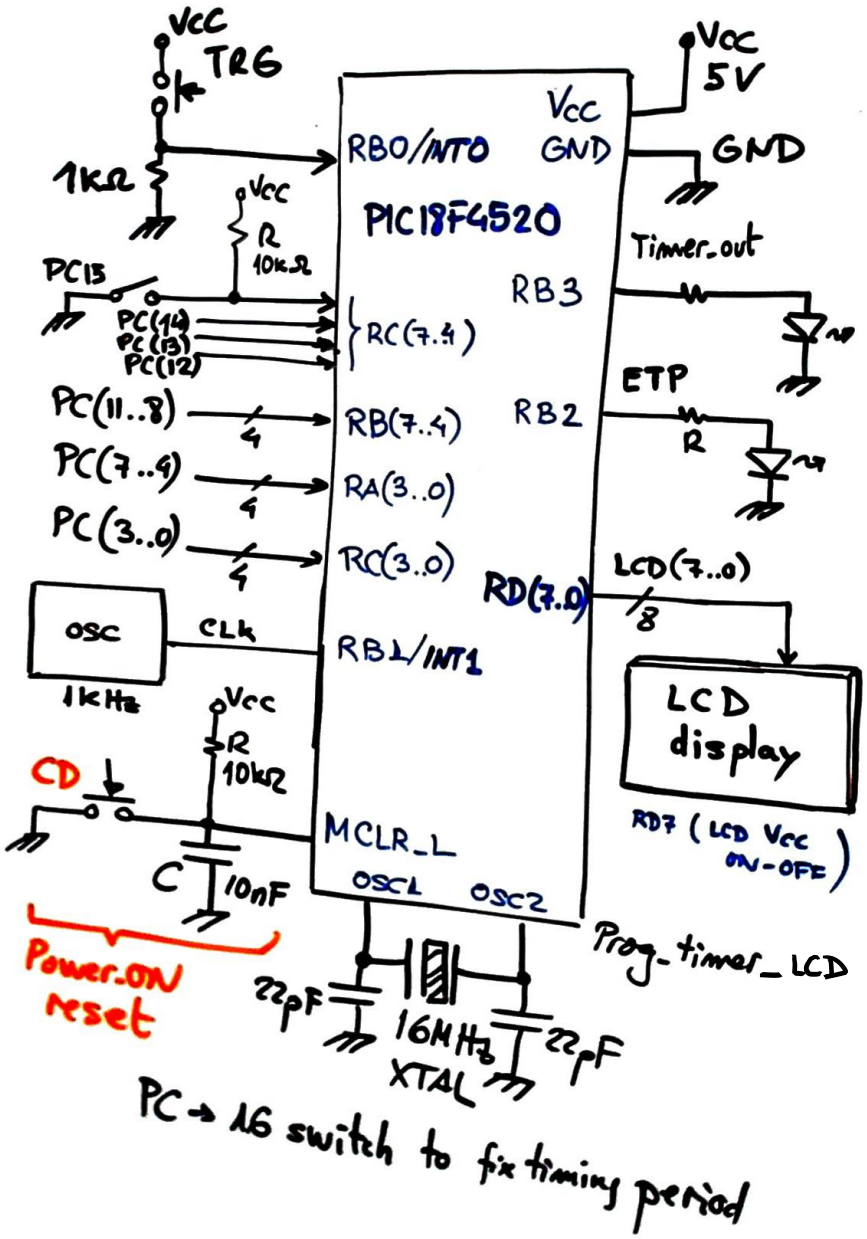

Fig. 2 Hardware circuit for the design phase #2 that includes the LCD display.

Subprojects planning related to lab sessions:

- Lab 9: SP3_1 (November 30th) is used to comprehend how basic I/O works. *init system()*, *read_inputs()*, *write_outputs()*. We will design a combinational circuit such *Comp_4bit* **(Work assessment December 14th)**.

- Lab 10: SP3_2 (December 14th), design phase #1, *Prog_Timer*, is used to implement the FSM and counter and datapath **(Work assessment December 21st)**.

- Lab 11: SP3_3 (December 21st), design phase #2, *Prog_Timer_LCD*, is used to add an LCD for printing messages (and even numerical data).

The complete design P_Ch3 will include the replacement of the external CLK by the internal peripheral TMR0 (design phase #3), *Prog_Timer_LCD_TMR0*, and the complete report and video presentation. Compare features with the programmable timer designed in P_Ch2. **(P_Ch3 due date: January 11th report + video submissions).**

III. Development & Test

The development and test of P_Ch3 implies solving each subproject beforehand and the final programing in C language of the complete system *Prog_Timer_LCD_TMR0.*

Testing is interactive using Proteus while programming and debugging C code step by step.

VERY IMPORTANT NOTE: Solving these laboratory assignments requires studying ahead and in group in detail similar examples and tutorials in CSD *digsys*.

Marking grids:

Work assessments (4p.):

SP3_1 14-12	SP3_2 21-12		P_Ch3 (Video) 11-01
1p	1p		2p

Handwritten report (6p.):

SP3_1	SP3_2	SP3_3	P_Ch3
1p	1p	2p	2p