CSD laboratory P_Ch1: 9-bit arithmetic unit

SP1.4 Designing a standard arithmetic circuit type 74LS85 using hierarchical structures and completing P_Ch1

I. Specifications of Comp_9bit

The aim of this preparatory laboratory assignment is to invent a 9-bit radix-2 comparator (*Comp_9bit*) using hierarchical structures based on components *Comp_1bit*. In this way, you can practise how to develop plan C2 and complete this component to be used in P_Ch1 as Chip2.

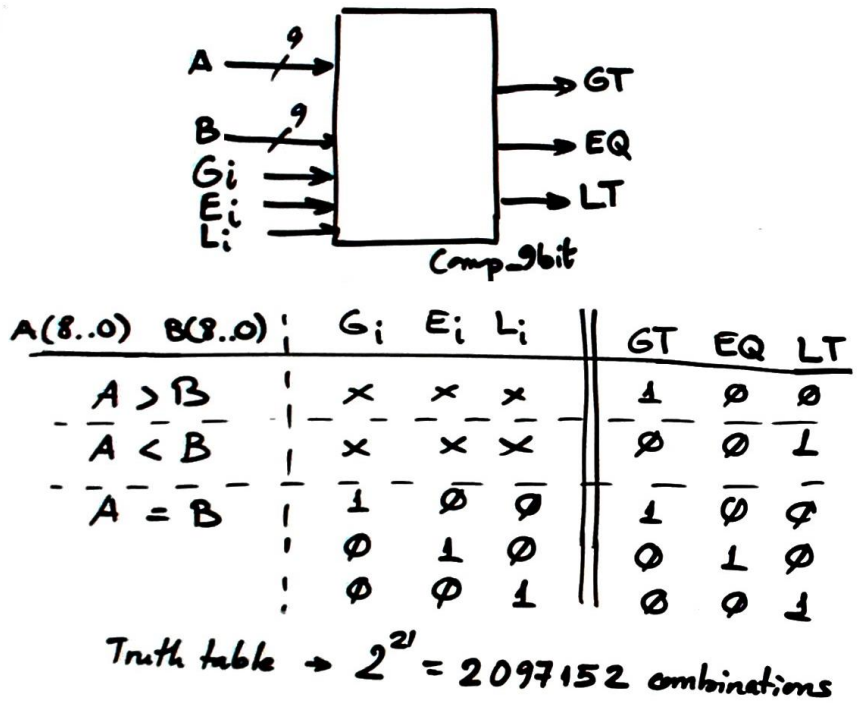

Fig. 1 *Comp_9bit* symbol.

II. Plan C2 using components and signals.

Draw a schematic plan C2 for the *Comp_9bit* using *Comp_1bit* components and logic if necessary.

III. Development. Synthesis.

Translate to VHDL the plan and write the *Comp_9bit.vhd*. Run a synthesis project and examine RTL and technology schematics.

Target chip: MAX II EPM2210F324C3 or Cyclone IV EP4CE115F29C7N

.

IV. Test and verification using VHDL testbench.

Organise a VHDL testbench *Comp_9bit_tb.vhd*. Run a ModelSim functional simulation and examine results from logic analyser to determine whether the circuit works as expected.

Completing P_Ch1

I. Specifications of *Arith_9bit*

Complete P_Ch1 using Chip1, Chip2 and Chip3 and all their internal components in Fig. 2 reporting all the previous subprojects and recording a video explaining how such hierarchical circuit is developed and tested.

II. Planning

The schematic plan of the P_Ch1 is already represented in Fig. 2.

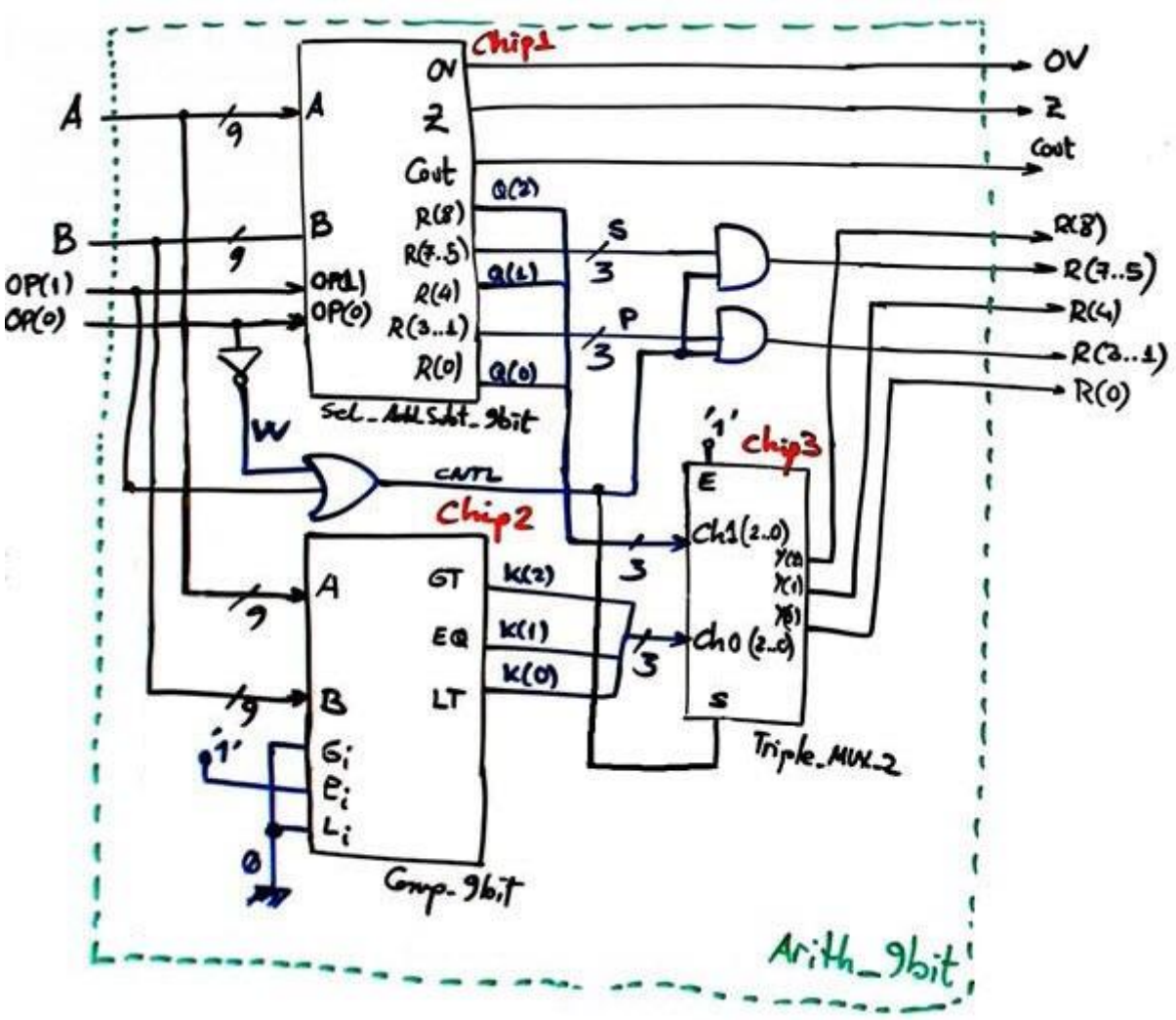

Fig. 2 Top architecture for P_Ch1 arithmetic unit. How many VHDL files contains this project?

III. Development. Synthesis.

Translate to VHDL the plan in Fig. 2 and write the *Arith_9bit.vhd*. Run a synthesis project and examine RTL and technology schematics.

Target chip: MAX II EPM2210F324C3 or Cyclone IV EP4CE115F29C7N

IV. Test and verification using VHDL testbench.

Organise a VHDL testbench *Arith_9bit_tb.vhd*. Run a ModelSim functional simulation and examine results from logic analyser to determine whether the circuit works as expected.