CSD laboratory P_Ch1: 9-bit arithmetic unit

SP1.3. Designing a combinational circuit using VHDL tools

1. Specifications

The aim of this laboratory project is to invent a 2-bit adder (*Adder_2bit*) using EDA tools (synthesis and simulation).

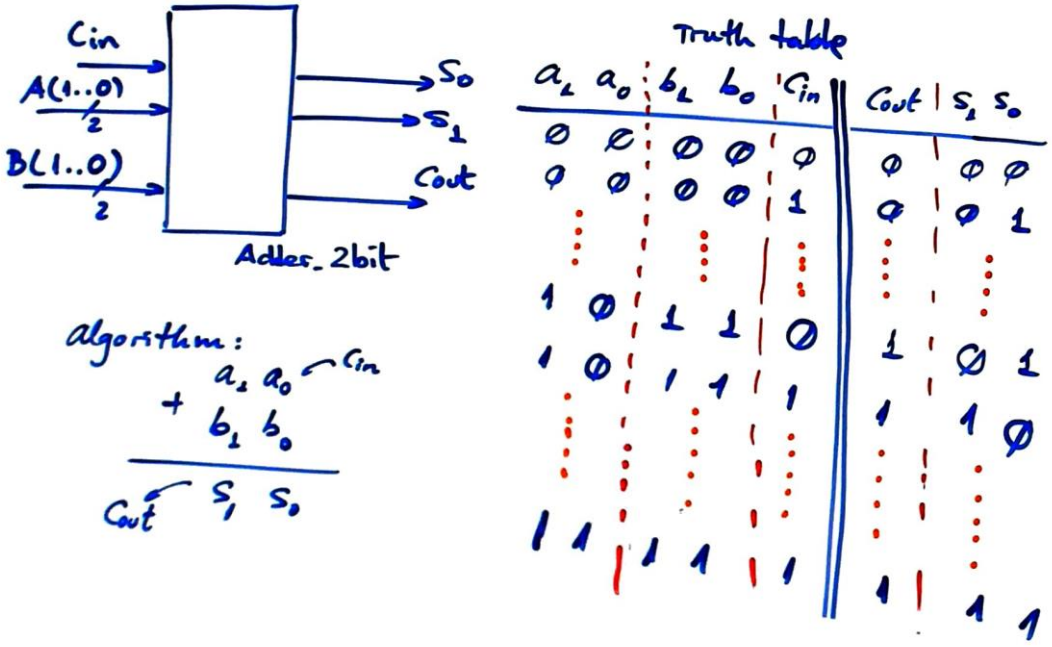

Fig. 1 *Adder_2bit* symbol and some truth table vectors.

- Complete the circuit truth table.
- Draw an example of timing diagram.

2. Plan
   I. Structural based on logic equations and gates. Example tutorial.
   II. Behavioural based on a high-level description of the circuit's truth table. Example tutorial.

3. Development. Synthesis.
   Target chip: MAX 10 10M50DAF484C7G. Discuss the schematics, explain differences and similarities
   A. Plan A → RTL and technology view.
   B. Plan B → RTL and technology view.

4. Test and verification using VHDL testbench.
   Verify that both plans are working as expected using the same testbench.