CSD laboratory P_Ch1: 9-bit arithmetic unit

SP1.2 Analysis of a circuit based on gates using VHDL (analysis method IV)

The aim of this laboratory exercise is to analyse *Circuit_SP1_1* to obtain its truth table[i] using EDA tools.

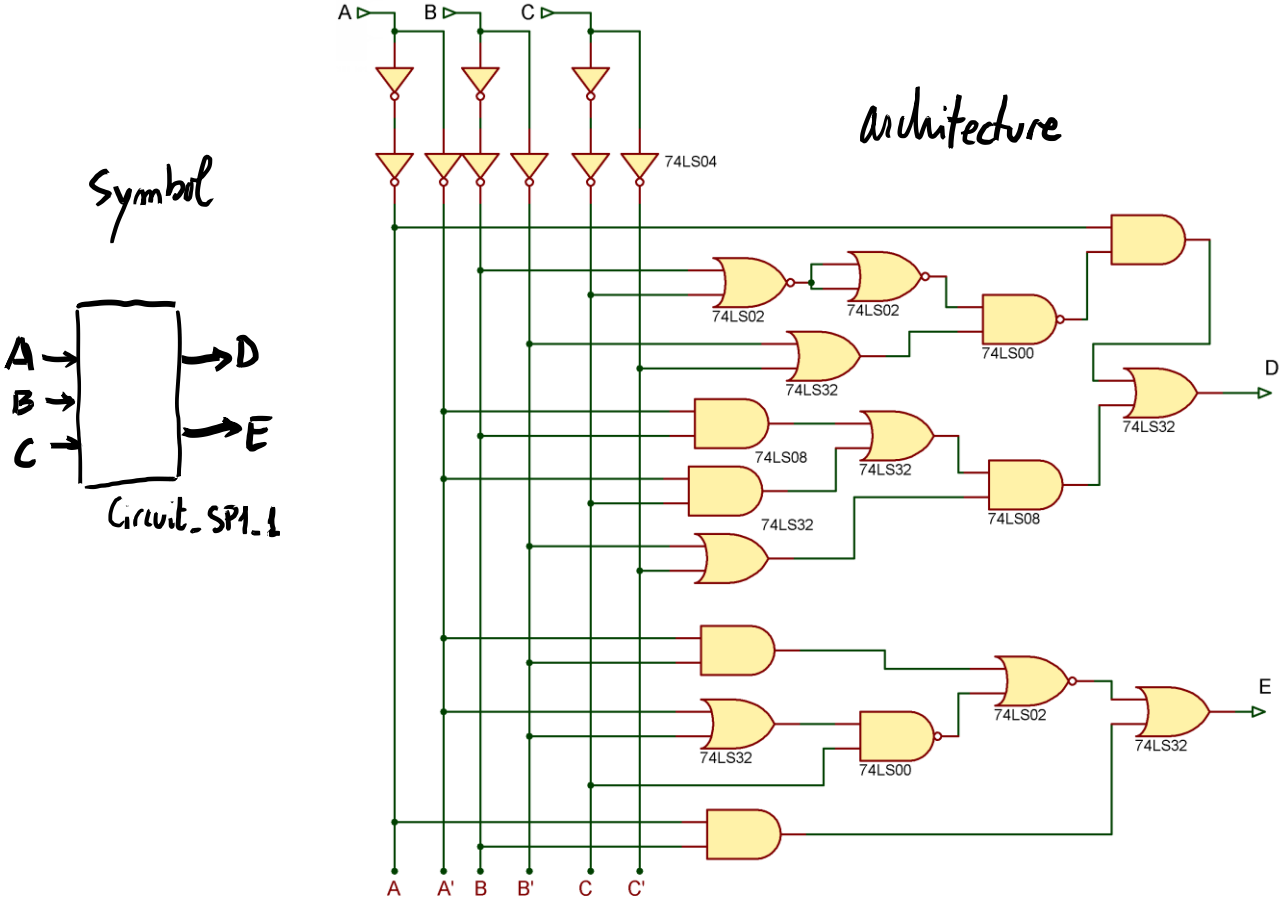

Fig. 1 Circuit *Circuit_SP1_1* to be analysed.

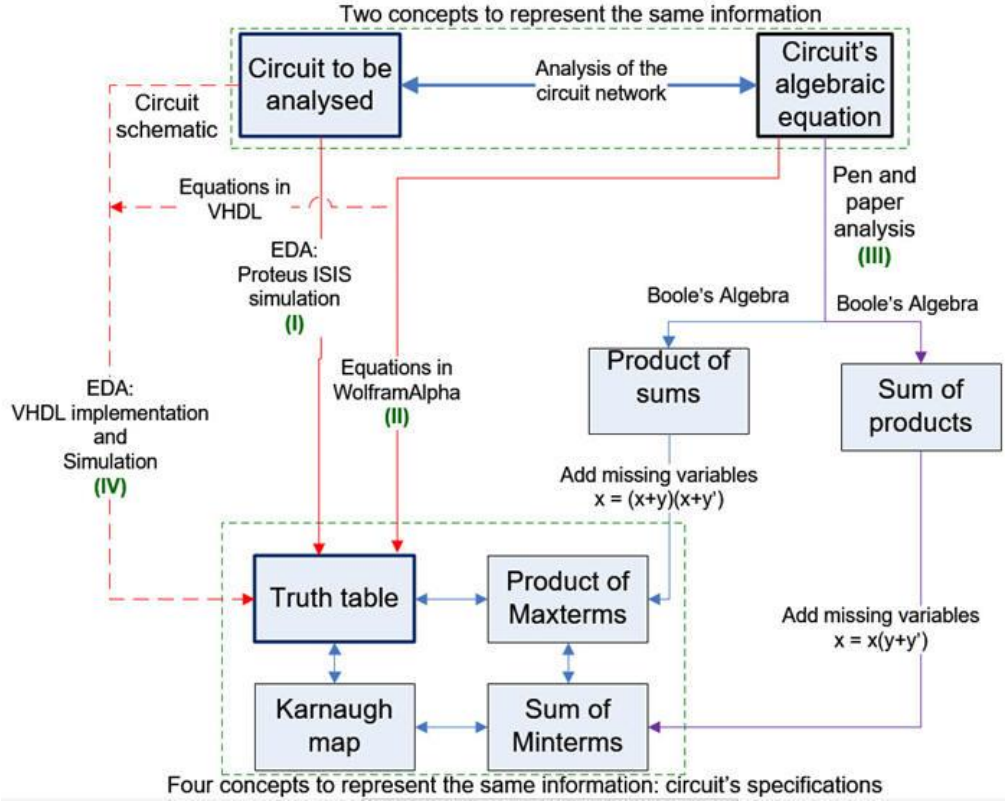

Fig. 2 Four strategies for analysing a given circuit.

The analysis process that follows path number (IV) must include:

1. Deduce circuit general equations. D = *f*(A, B, C); E = *f*(A, B, C).

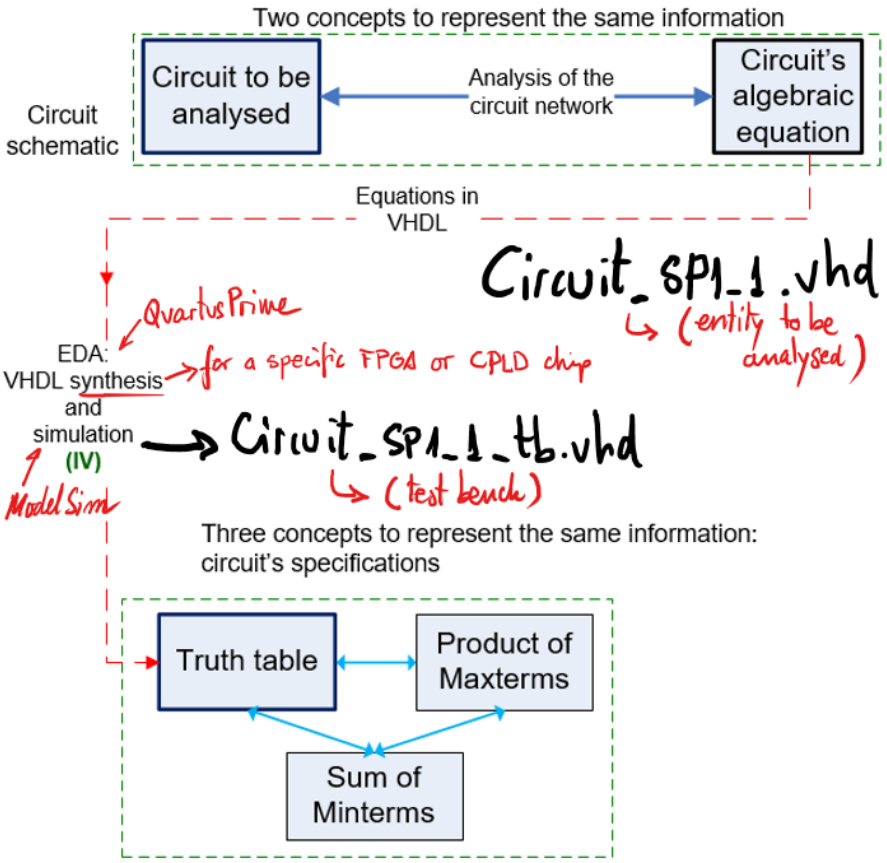

Fig. 3 Analysis method IV.

2. Write them in VHDL ***Circuit_SP1_1.vhd*** using an example file from the analysis section in this tutorial.

3. Start a Quartus Prime project for a target chip 10M50DAF484C7G from Intel.

4. Synthesise and view RTL and technologies schematics.

5. Generate a skeleton of a testbench and add all the truth table input vectors. Observe how this step is solved in this similar tutorial: ***Circuit_SP1_1_tb.vhd***

6. Start a ModelSim Intel Starter Edition project and simulate the testbench and the unit under test.

7. Using the wave logic analyser deduce the circuit truth table and compare results with other methods.

[i] This circuit is simply another implementation of the *Adder_1bit* solved in P3 by means of different plans.