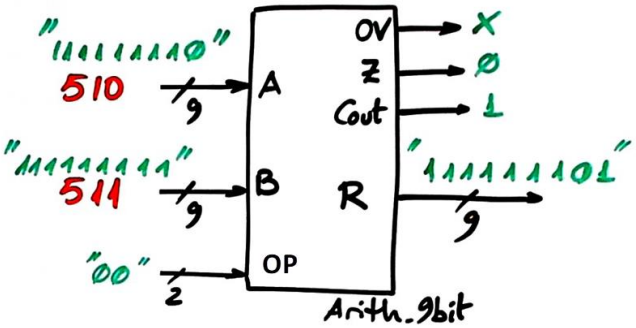
**CSD laboratory P_Ch1: 9-bit arithmetic unit**

## I. Specifications

The aim of this project is to invent a chip capable of performing arithmetic operations. Fig. 1 shows the chip symbol and an example of input and output vectors when OP = "00". This project is aimed at Intel Cyclone IV EP4CE115F29C7 FPGA target chip.




| OP | Operation | |
|---|---|---|
| 00 | Add in radix-2 | A+B |
| 01 | Compare in radix-2 | (A>B), (A=B), (A<B) |
| 10 | Add signed integers | A+B |
| 11 | Subtract signed integers | A-B |

Fig. 1 *Arith_9bit* unit to design and table of operations.

## II. Planning

This chip can be designed internally using many strategies. To make it simple, we propose a given architecture represented in Fig. 2 based on a hierarchical structure of components and signals. Chip1 is a 9-bit selectable adder subtractor to work with radix-2 and integer numbers for performing "00", "10" an "11" operations. Chip2 is a radix-2 9-bit comparator. Plan and develop Chip1, Chip2 and Chip3 before building the top entity.

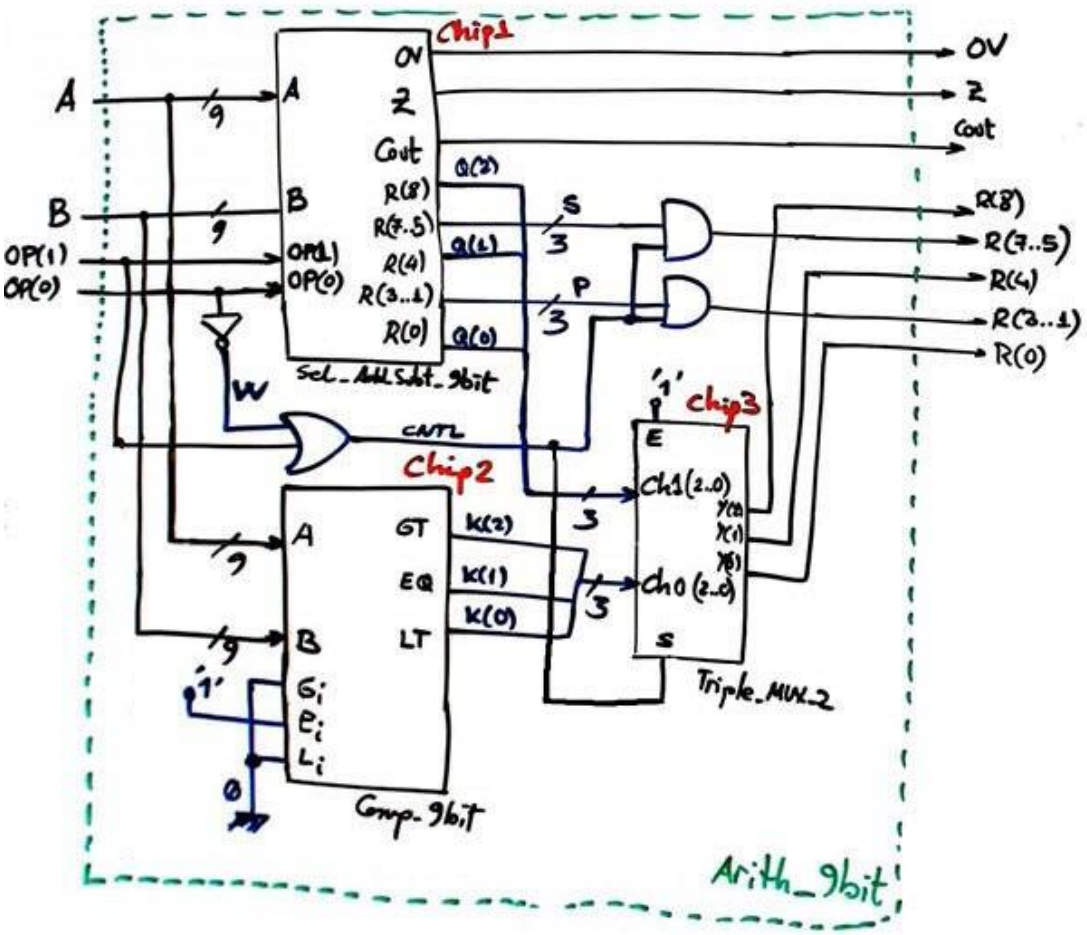



Fig. 2 *Top level internal architecture for the Arith_9bit.*

Subprojects planning:

- SP1.1 is used to comprehend how an Adder_1bit works **(Work assessment September 28th)**.
- SP1.2 is used to build start working with VHDL EDA tools for synthesis and simulation **(Work assessment October 5th)**.
- SP1.3 is used to practise with flat (single-file) VHDL projects **(Work assessment October 19th)**.
- SP1.4 is used to practise with hierarchical (multiple-file) VHDL projects and for designing Chip2. At the same time this SP1.4 completes P_Ch1 as represented in Fig. 1 **(Due date: October 26th)**

III. Development.

The development of P_Ch1 implies completing each subproject beforehand and the final construction in VHDL of the circuit in Fig. 2.

IV. Test and verification

Testing P_Ch1 implies testing each project beforehand and the final verification of the circuit in Fig. 2 using several test vectors and operations.

## Marking grids:

Work assessments (3p) to be carried out in laboratory sessions:

| SP1.1 **28-09** | SP1.2 **05-10** | SP1.3 **19-10** |
|---|---|---|
| 1p | 1p | 1p |

P_Ch1 handwritten report (6p) and video presentation:

| P_Ch1 **26-10** | | | | |
|---|---|---|---|---|
| Annexed materials in P_Ch1 report (see note below) | | | | P_Ch1 video |
| SP1.1 | SP1.2 | SP1.3 | SP1.4 | |
| 1p | 1p | 2p | 2p | 1p |

NOTE on submissions

**Report.** Example of P_Ch1 written report layout (one submission per cooperative lab group), a single PDF file:

1. Specifications and theory

Original handwritten materials on symbol, truth table, timing diagram and other explanations on data times and operations to be performed.

2. Planning

Original handwritten explanations and VHDL-ready schematics on how this plan C2 circuit is conceived, proposed hierarchy of components, signals, number of VHDL files, project folders and names, etc.

3. Development

Project in Quartus Prime for a target FPGA chip: Intel Cyclone IV EP4CE115F29C7.
Printing and discussion of RTL and technology schematics. How many FPGA resources (LOGIC_CELLS) are used?

4. Test and verification

Testbench schematic, proposed stimulus testbench process, printing and discussing results.

5. Annexes

Add here work done in previous weeks and assessed in work in process. Basically projects on designing components to be used in this *Arith_9bit* like the Comp_9bit (SP1_4).

**Video** presentation: 10 min. max., 3 -4 min. each participant.

The idea of the video presentation is different from the report and has its own particular objective: develop your oral communications skills in this engineering context.

No need to explain every single detail of every project or exercise you've been solving for more than a month, but start putting in motion your communication skills that you'll continue to practise and improve through P_Ch2 and P_Ch3.

Therefore, you can choose something to explain: a component, a subproject, or the complete *Arith_9bit* in P_Ch1, because we'll focus assessment (1/10) in how you are organising the presentation, how confident you are in front of the camera, time sharing among students, support materials, time distribution and audio and video quality.