CSD laboratory P_Ch2: Programmable timer

I. Specifications

The aim of this project is to invent a digital programmable timer.

Features:

- Programmable 24-bit pulse count (**PC**)
- 16 MHz external **CLK** reference (T_{CLK} = 62.5 ns)
- End of timing period pulse (**ETP**) flag (width T_{CLK})
- Active-high larger than 70 ns trigger **TRG** pulse
- Asynchronous reset.
- Timed output signal **Timer_out** = PC · T_{CLK} (maximum timing period = 1.048576 s)
- Intel Cyclone IV EP4CE115F29C7N FPGA target chip
- Dedicated processor architecture.

Fig. 1 shows the chip symbol and an example of typical waveforms.

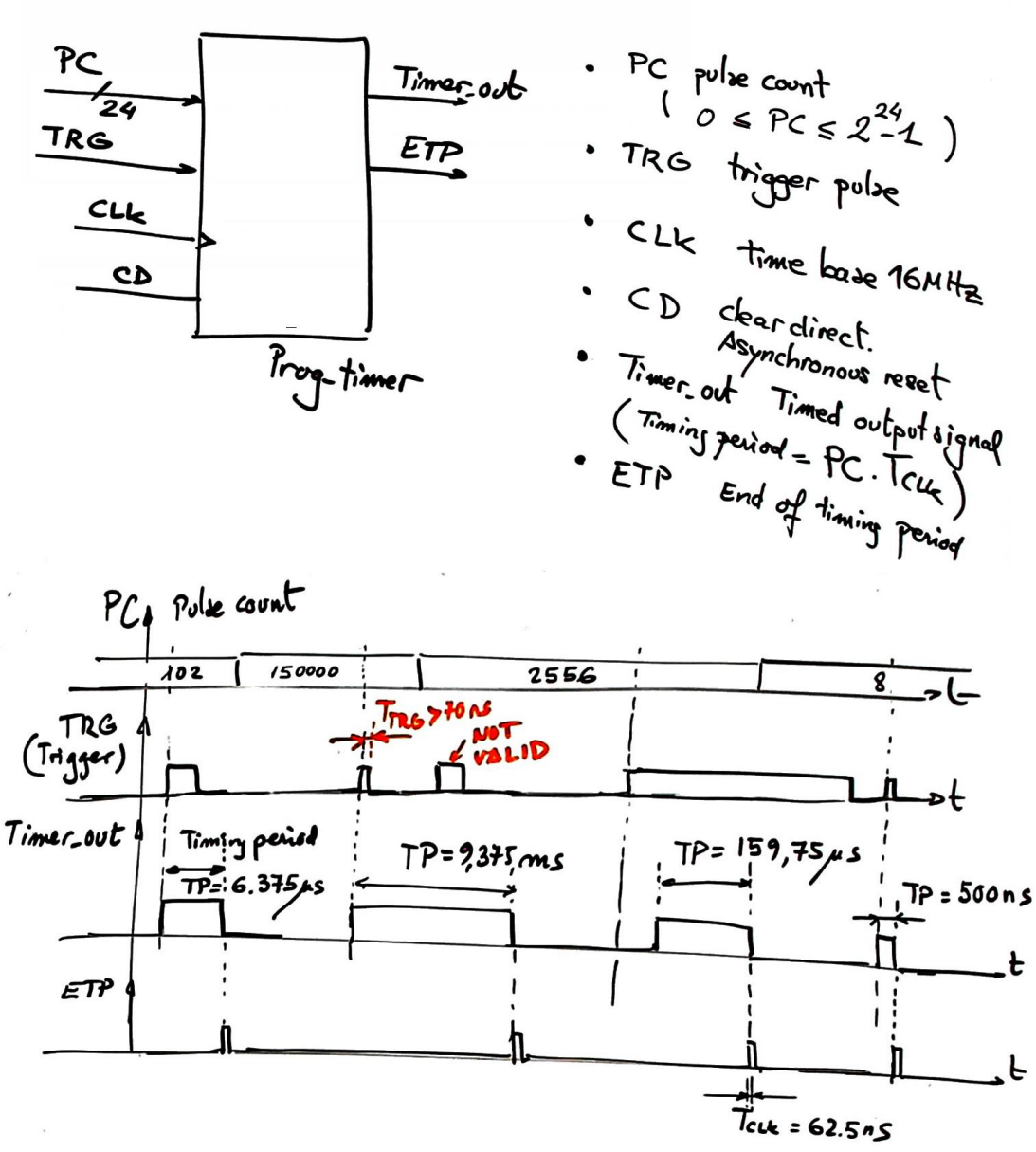

Fig. 1 Symbol and typical waveforms. A pulse, for instance clicking a button, triggers the timing period. Once the timing period (TP) ends, a single pulse of T_{CLK} duration is generated to indicate that the device is idle and can be used again for programing any other timing interval. This device is non-retriggerable, meaning that other trigger pulses are ignored while the device is on duty.

A timer is a system that is used widely in industrial, manufacturing, telecommunications and aerospace applications. For instance, to name a few: staircase, irrigation, time lock, kitchen (egg timer), TV sleep function, watchdog, pulse generator, countdown, call timer, delay generator, timed switch or outlet, auto power off functions, energy saving systems, motor drivers and process sequencers, etc. Timers also become subsystems of many precision scientific instrumentation such as frequency meters or signal generators. Timers may be non-retriggerable or retriggerable, and may include a keypad to program timing period and 7-segment or LCD display to show current time count. Since the function of counting is very similar to timing, the programmable timer can be easily configured to operate as timer or as counter. This feature provides industry the ability to purchase and stock one device for use as a timer or counter. This double functionality will be studied in PIC18F microcontroller TMR0 in P12.

II. Planning

This chip can be designed internally using many strategies. To make it simple and reasonable in the given time constraints, and to be able to embed its design within CSD course timeline, we propose a given architecture represented in Fig. 3 based on the generalised dedicated processor architecture in Fig. 2

We intent to adapt this circuit to microcontrollers in P_Ch3 empowering you to compare design features and product performance from both technologies: digital hardware based on FPGA and microcontrollers.

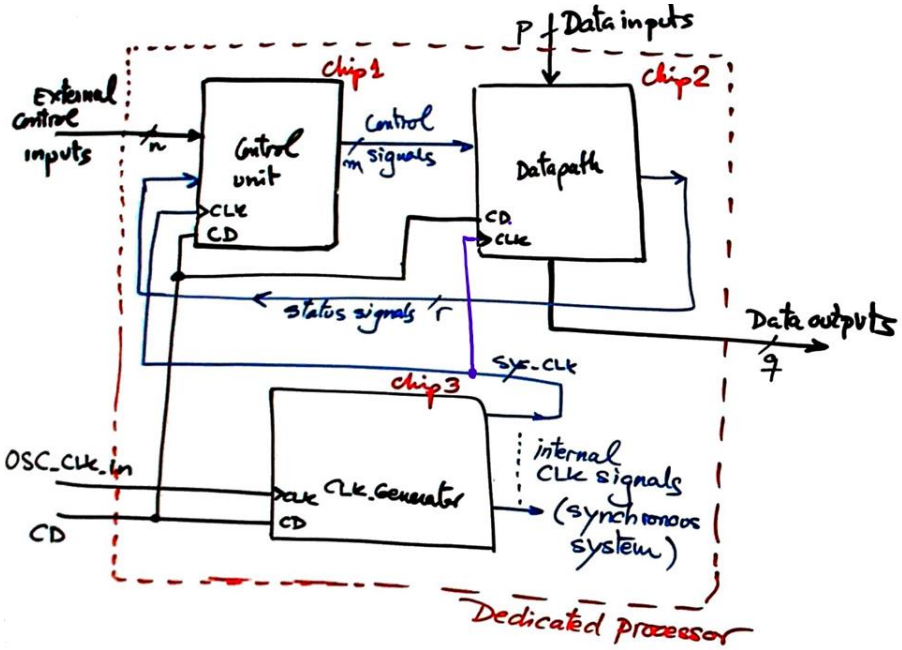

Fig. 2 General architecture of an advanced digital system or dedicated processor to solve a specific function or algorithm. Data inputs are information or signals to be processed by the device. In our project, the physical quantity to be processed is *time*; we intent to generate a pulse which time duration depends on pulse count (PC) and time base represented by the CLK signal. In our project, Chip3 is not used, and thus our information processor consist of Chip1 (control unit: FSM), and Chip2 (datapath or operation unit: registers, counters, memory cells, combinational circuits, etc.).

Subprojects planning related to lab sessions:

- Lab 4: SP2_1 is used to comprehend how to perform propagation delay measurements, gate-level simulations, timing analyser and circuit speed calculations. We will measure such parameters for the *Comp_9bit* from P_Ch1 (P_Ch2 requires a *Comp_24bit* in the datapath) **(Work assessment November 9th)**.

- Lab 5: SP2_2 is used to discover how 1-bit memory cells work analysing a *Circuit_type7493* based on flip-flops. Two circuits will be given for comparison: asynchronous and synchronous. **(Work assessment November 16th)**.

- Lab 6: SP2_3 is for implementing the system control unit Chip 1 as a canonical synchronous FSM. State diagram will be given as initial data because the project emphasis is placed on translating FSM into VHDL. A testbench schematic and its VHDL files will be supplied in order to test the control unit. **(Work assessment November 23rd)**.

- Lab 7: SP2_4 is used to discuss how counters and registers are implemented in VHDL. Datapath's Chip2 and Chip3 will be given as initial resources and discussed in detail, so that the aim will rely on connecting hierarchical structures following plan C2 and completing P_Ch2. **(P_Ch2 due date: November 30th. Report + video submissions).**

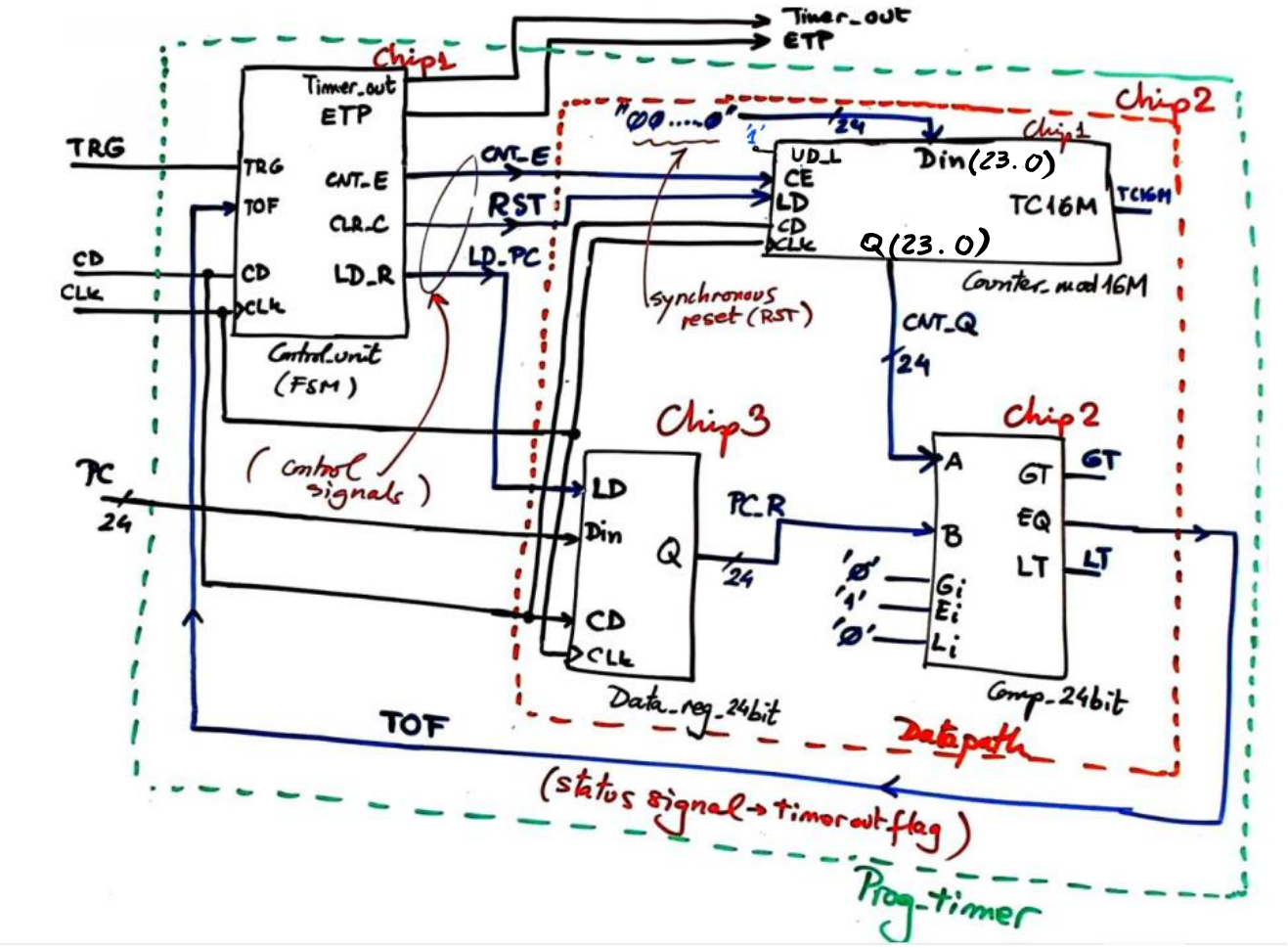

Fig. 3 Top level internal architecture for the *Prog_Timer*. Datapath components allow counting CLK pulses and generating status signals for the control unit.

III. Development.

The development of P_Ch2 implies completing each subproject beforehand and the final construction in VHDL of the system *Prog_timer* in Fig. 3.

IV. Test and verification

Testing P_Ch2 implies testing SP2_1, SP2_2 and SP2_3 projects beforehand and the final verification of the circuit in Fig. 3 using several trigger signals and pulse count values.

VERY IMPORTANT NOTE: Solving these laboratory assignments requires studying ahead and in group in detail similar examples and tutorials in CSD *digsys*.

Marking grids:

Work assessments (4p.):

SP2_1 **09-11**	SP2_2 **16-11**	SP2_3 **23-11**	SP2_4 **30-11** (Video)
1p	1p	1p	1p

Handwritten report (6p.):

SP2_1	SP2_2	SP2_3	SP2_4
1p	1p	2p	2p