SP2_4 Designing datapath components and assembling the programmable timer

Design the datapath components and complete, develop and test the programmable timer in Fig. 1.

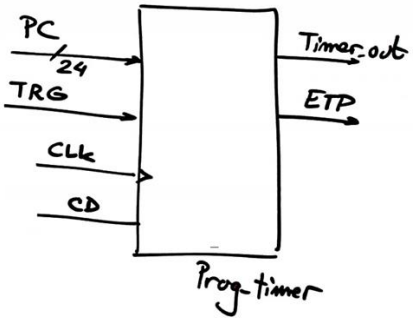

Fig. 1. Symbol

Follow the sequence below to complete this project:

1. Implement *Comp_24bit* from SP1_4 or SP2_1.
2. Use the tutorial on plan Y large counters to implement *Counter_mod16M*.
3. Use the tutorial on data registers to implement *Data_reg_24bit* (or use again the same *Counter_mod16M* as a data register.
4. Build the *Datapath* component and synthesise it.
5. Combine the *Datapath* and the FSM in SP2_3 to implement the *Prog_Timer*. Synthesise it and test the project using both functional and gate-level simulations triggering several times the device for different pulse count (PC) values.

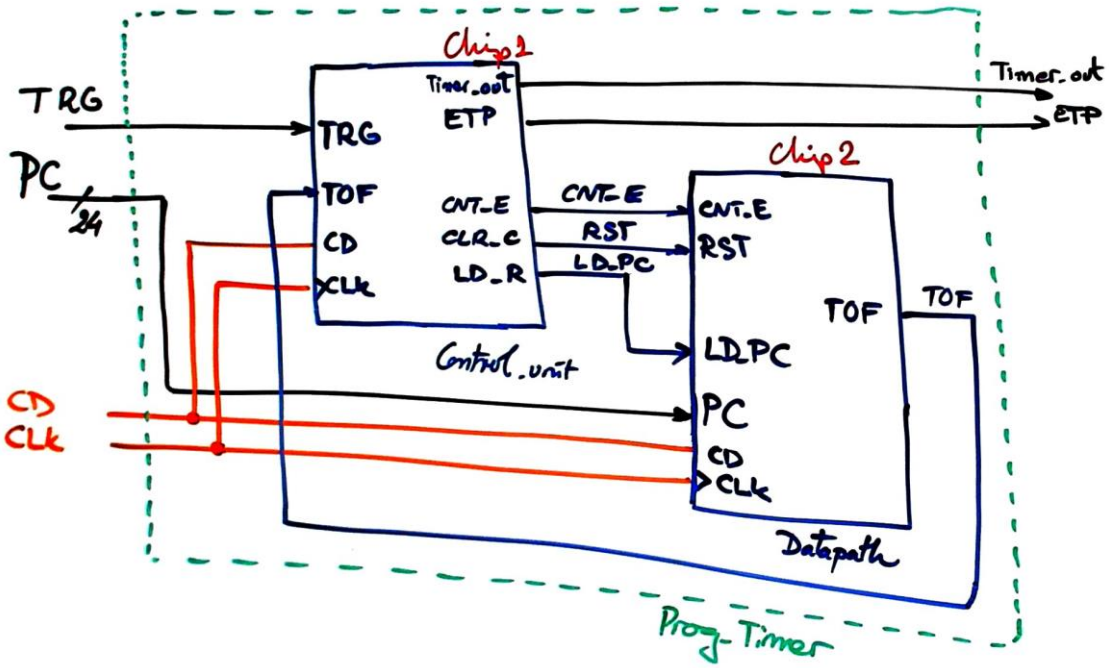

Fig. 2. Programmable timer designed with an internal architecture as a dedicated processor.