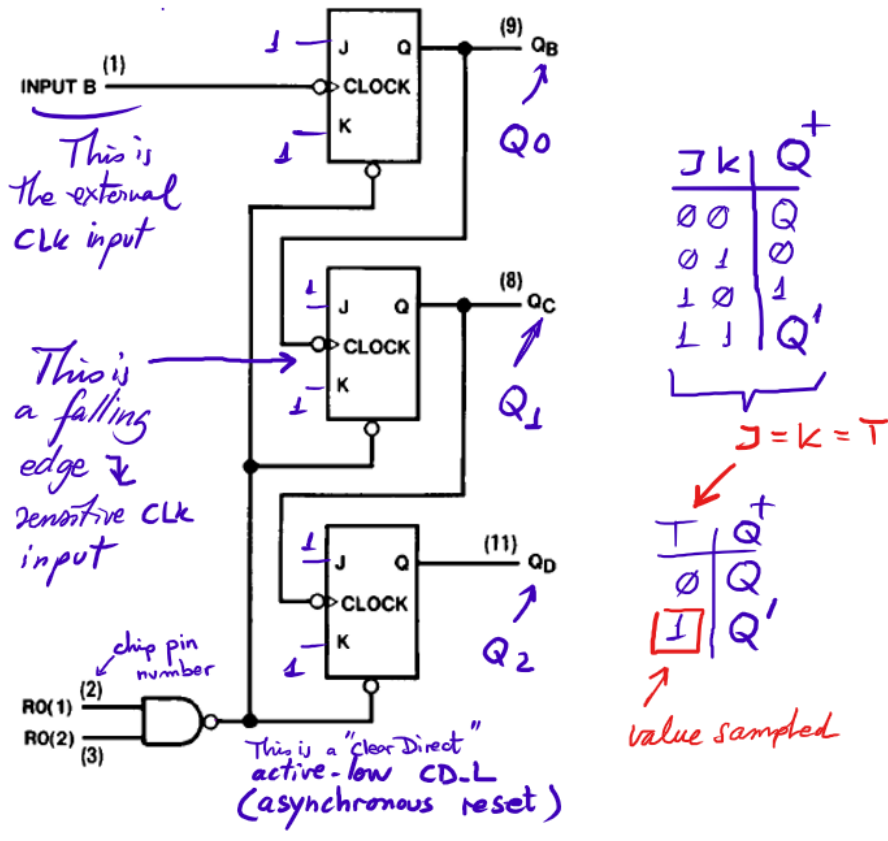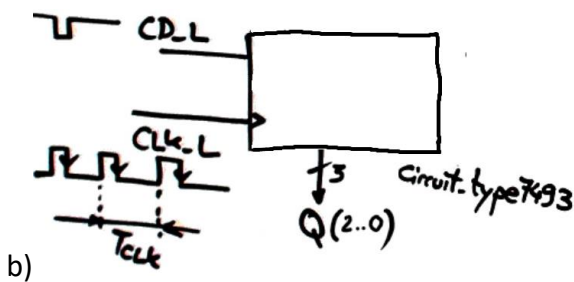# CSD laboratory P_Ch2: Programmable timer

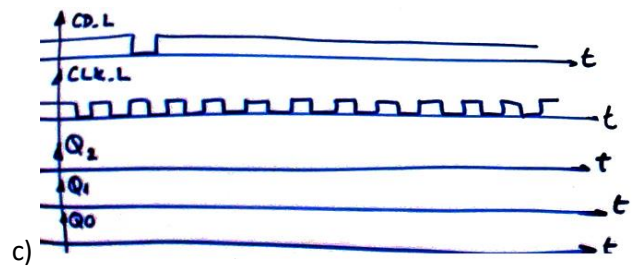## SP2_2 Analysis of a circuit based on flip-flops

This lab exercise is similar to the problems proposed in P5. Analyse using three methods the circuit based on Flip-flops extracted from 74LS93A chip represented in Fig. 1.
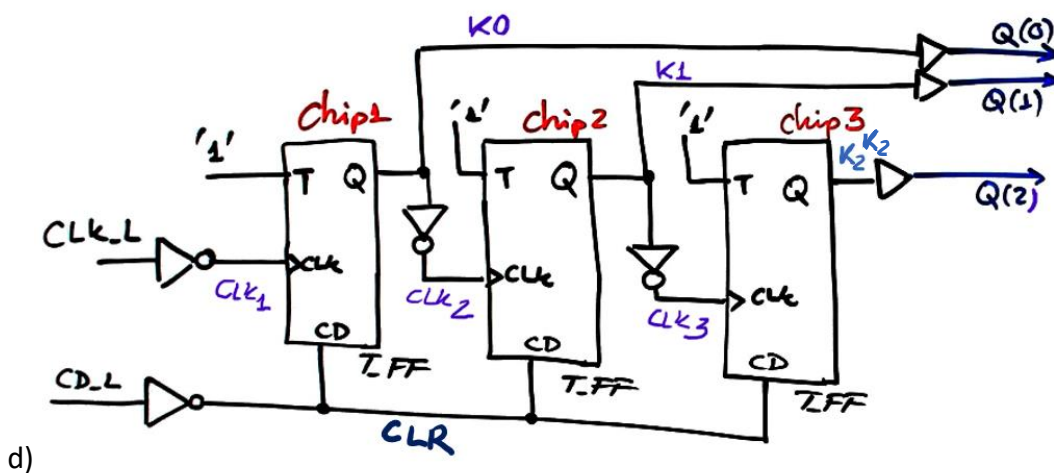

a)

b)

c)

d)

Fig. 1 *Circuit copied from 74LS93A commercial chip and adapted to our conventions.*

1. Analyse the circuit in Fig 1 drawing a timing diagram sketch to see how each flip-flop evolves in time. Determine what kind of output codes are generated each CLK cycle. What is the function of this circuit?

2. Capture the circuit in Proteus and run simulations to check whether your paper analysis is correct. Use the logic analyser instrument to represent both inputs and outputs in function of time. Use this circuit to adapt.

3. Capture the circuit in VHDL as a plan C2 structure, synthesise it and run a simulation testbench to represent all inputs and outputs in time in a wave timing diagram. You can use as you like *JK_FF* or *T_FF* as components. What is the maximum CLK frequency when picking a target chip MAXII EPM2210F324C3?

Optional this second circuit for comparison and further discussion

Fig. 2 represents a circuit based on *D_FF* found browsing Internet. Let us name it *Circuit_DFF*. We have adapted it as usual to our conventions and naming style so that we can use our set of tools to analyse it. Input *Enable* is not necessary because it is simply a CLK blocker when '0' preventing the circuit advancing in time (in P7 we will present better methods for halting, stopping or freezing a circuit activity without interfering CLK signal). Determine how does the circuit work, meaning finding the vector output Q(2..0) using the three methods:

1. Handwritten analysis.
2. Proteus capture and simulation.
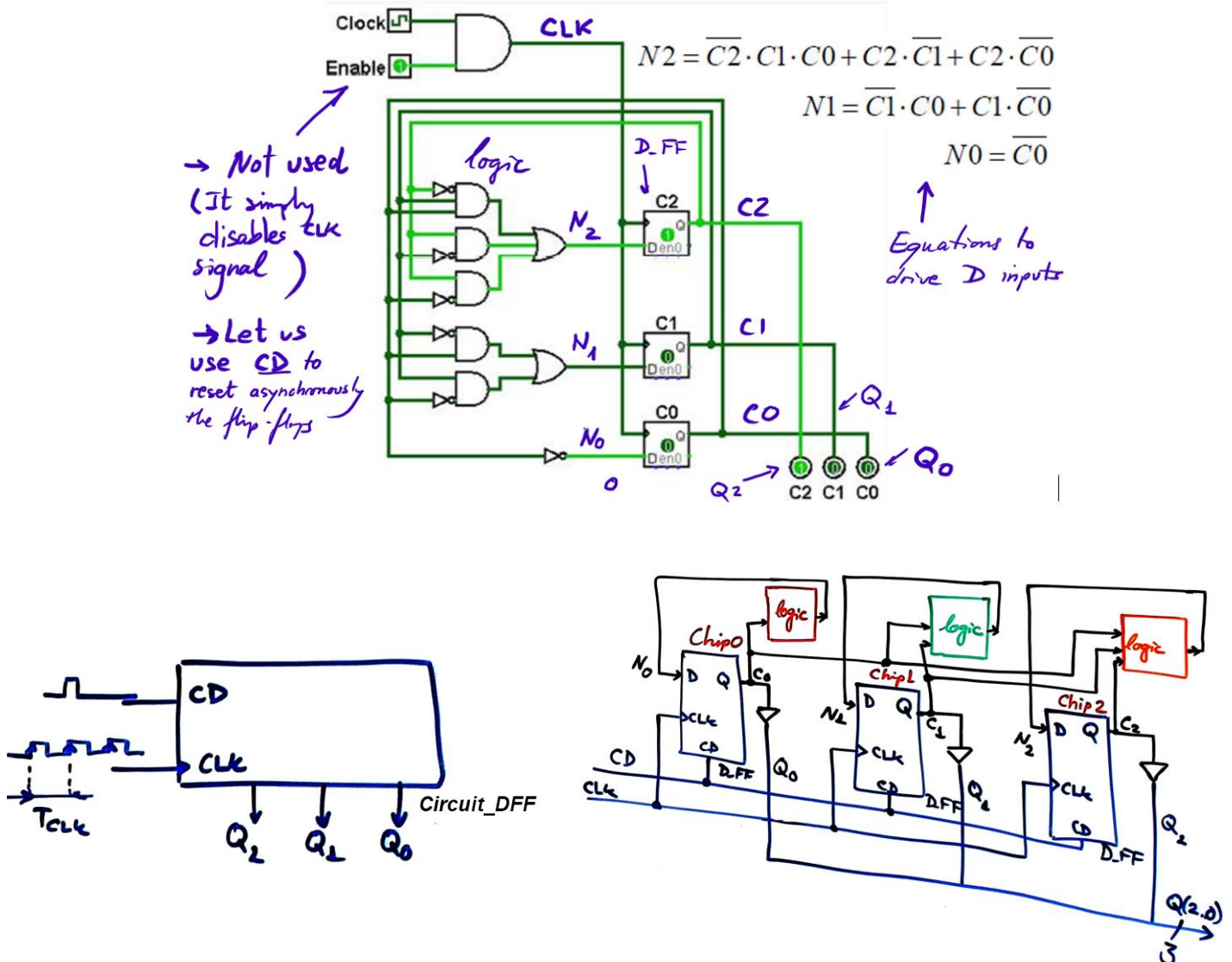3. VHDL synthesis and test. What is the maximum CLK frequency when picking a target chip MAXII EPM2210F324C3?

$$N2 = \overline{C2}\cdot C1 \cdot C0 + C2 \cdot \overline{C1} + C2 \cdot \overline{C0}$$

$$N1 = \overline{C1}\cdot C0 + C1 \cdot \overline{C0}$$

$$N0 = \overline{C0}$$

Equations to drive D inputs

Fig. 2 Circuit_DFF *to be analysed using several tools*