SP2_1 Measuring and calculating *Comp_9bit* processing speed (step 5 in our design flow)

(NOTE: Sections I, II, II, and IV are already solved in SP1_4, so this subproject is the continuation section V. Be sure that these preliminary sections from I to IV are solved correctly before attempting section V)

I. Specifications of *Comp_9bit*

The aim of this preparatory laboratory assignment is to invent a 9-bit radix-2 comparator (*Comp_9bit*) using hierarchical structures based on components *Comp_1bit*. In this way, you can practise how to develop plan C2 and complete this component to be used in P_Ch1 as Chip2.

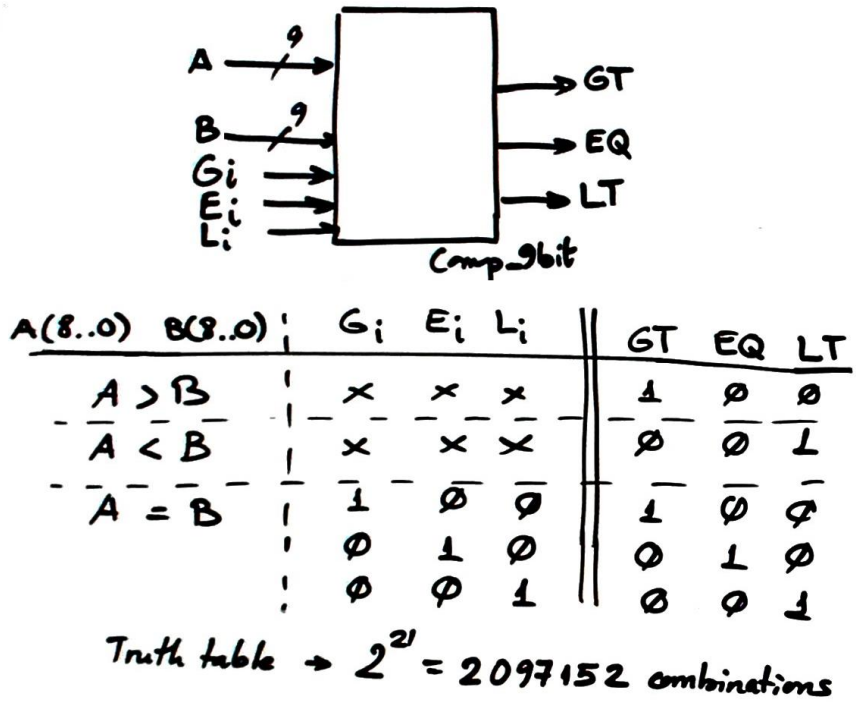

Fig. 1 *Comp_9bit* symbol.

II. Plan C2 using components and signals.

Draw a schematic plan C2 for the *Comp_9bit* using *Comp_1bit* components and logic if necessary.

III. Development. Synthesis.

Translate to VHDL the plan and write the *Comp_9bit.vhd*. Run a synthesis project and examine RTL and technology schematics. Synthesise the circuit for a **Cyclone IV EP4CE115F29C7N** FPGA target chip.

IV. Test and verification using VHDL testbench.

Organise a VHDL testbench *Comp_9bit_tb.vhd*. Run a ModelSim functional simulation and examine results from logic analyser to determine whether the circuit works as expected.

V. Technology view circuit verification using VHDL testbench.

- Run a ModelSim **gate-level simulation** and examine results from logic analyser to determine whether the circuit works as expected in several signal transitions. How long does it take to reach the correct value?
- Run Quartus Prime **timing analyser** tool and examine spreadsheets to determine the worst-case scenario
- Calculate the maximum number of operations per second that Comp_9bit is capable of performing.

Repeat measurements for a **MAX II EPM2210F324C3** CPLD target chip and compare results.

Optional in this P_Ch2_SP1

Build the 24-bit radix-2 comparator *Comp_24bit* required as Chip2 in timer datapath represented in Fig. 3 in P_Ch2. As usual in CSD, building a circuit means project steps 1 -2 -3 -4 -5 in order to design the component and leave it ready for use as a component in other designs.