## CSD laboratory P_Ch1: 9-bit arithmetic unit

### Subproject SP1.1 Analysis of *Circuit_SP1_1*

The aim of this laboratory exercise is to analyse *Circuit_SP1_1* in Fig. 1 to deduce its truth table using up to two methods from this concept map[1]: D = *f*(A, B, C) ; E = *f*(A, B, C)

- Method 1: Using Proteus and simulation models from the LS-TTL (Low-power Schottky Transistor–transistor logic) components library.
- Method 2: Using WolframAlpha

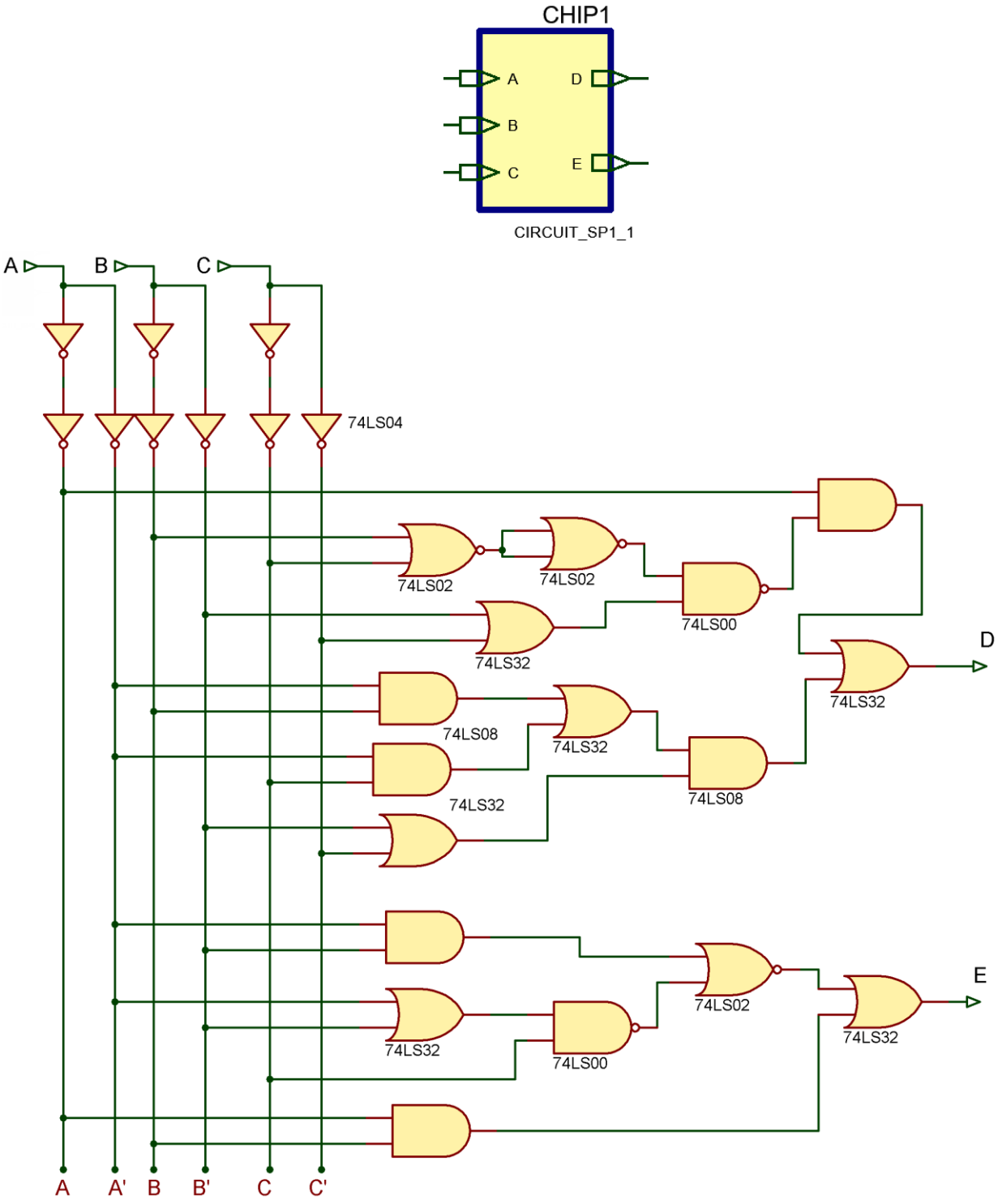


Fig. 1 *Circuit_SP1_1* composed of a network of logic gates.

[1] Method 3 can be used as an additional classroom exercise, and method 4 will be the subject of next SP1_2.