Project 1. Analysis of flip-flop circuits (5p)

A. Analyse the circuit in Fig. 1 and draw a timing diagram of the outputs Q(3..0). How many states does this circuit have? What is the output value **Q(3..0)** for each state, what HEX symbols is the circuit generating?

   - Identify CLK signals in the circuit. Is it asynchronous or synchronous? Go step by step in time (which means advancing by T_{CLK} periods (circuit's time resolution).

   - Be sure to identify correctly the sampled values of control inputs (T, D, J, K) at CLK's rising edges and thus be able to apply flip-flops' function tables. If necessary, consider the CLK to output propagation time (t_{CO}) in the range of ns associated to flip-flop output transitions.

   - Once the timing diagram finished, determine the number of states and binary output values for each state.

B. Verify your results by capturing and simulating the circuit in Proteus.

C. Verify your circuit using VHDL tools for synthesis and simulation (plan C2). How many flip-flops are identified in the technology view?

D. How fast is this circuit synthesised for a CPLD MAX II EPM2210F324C3 or for an FPGA Cyclone IV EP4CE115F29C7?

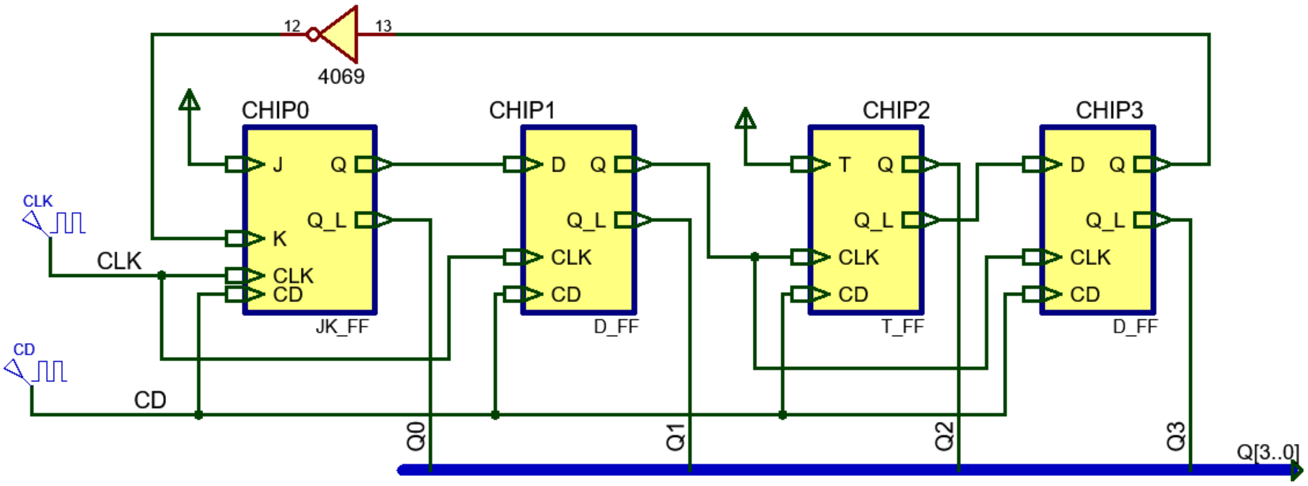
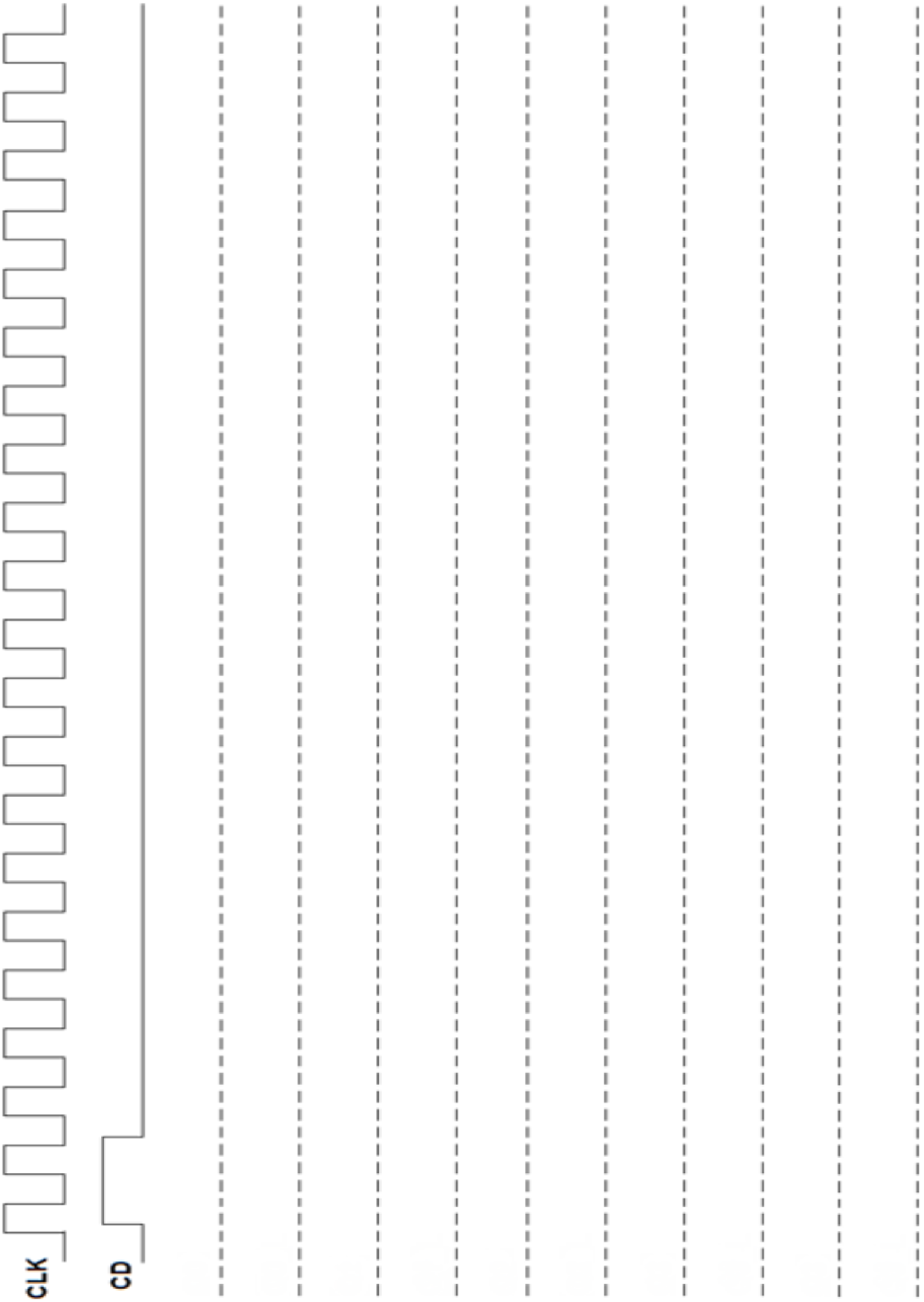


Fig. 1 Circuit based on flip-flops for introducing 1-bit memory cells and experimentation.

Marking grid:

A	B	C	D
3p	2p	3p	2p



Print this sheet as a template for deducing the timing diagram of the circuit.

Project 2. Designing a traffic light controller. (5p)

a. Specifications. Read interesting ideas and project details in this Wikipedia entry. We want to design a traffic light controller adapting the example shown in this former P6 tutorial. Fig. 2 reproduces the sketch where road car sensors, pedestrian buttons and traffic light poles are installed to control avenue A and street B intersection. Organise requirements and features so that the project can be implemented in three design phases 1, 2, 3.

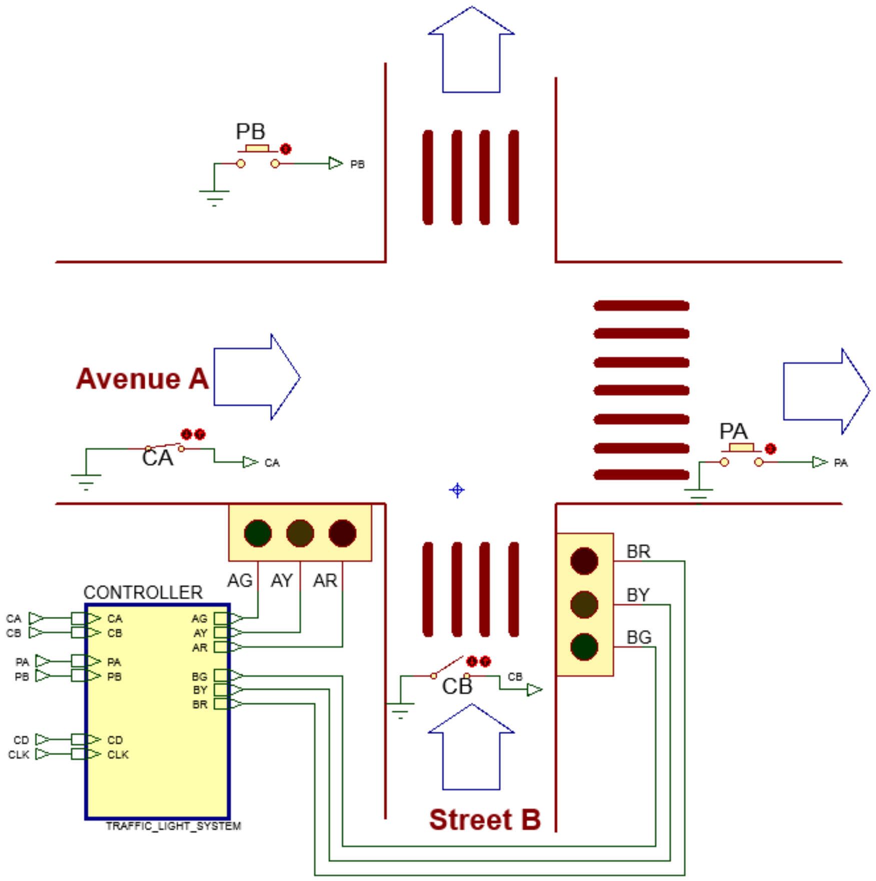


Fig. 2
Sketch of the street junction where to install our traffic light controller.

Plan, develop and **test only the phase 1** of the project.

b. Plan phase 1: FSM architecture with real-time light timer flag to allow lights sequencing and night mode. Draw the state diagram.

c. Plan: adapt the general FSM architecture to this problem and draw the state register based on D_FF. Deduce how many D_FF are required if you are coding in binary sequential or in one-hot.

d. Plan: write the truth table of CC1 and CC2 and their equivalent behavioural interpretations in flowcharts.

e. Development: write the VHDL file *Traffic_light_controllerr.vhd* by translating the flowcharts and the state register. Run a project using an EDA synthesis tool for a CPLD or FPGA target chip. Print and discuss the RTL and the technology schematics. The CLK oscillator is 1 MHz.

f. Test: simulate the circuit using a VHDL test bench and discuss the results. Measure the maximum CLK frequency that can be applied to your design considering a target chip from Lattice Semiconductor (ispMach4128V TQFP100), Intel (Cyclone IV EP4CE115F29C7), or Xilinx (Spartan-3E XC3S500E-FG320).

g. (optional) Demonstrate your design in an FPGA DE2-115 prototyping board.

Marking grid:

a	b, c, d	e,f
2p	3p	5p

For other advanced projects:
Phase 2: specifications, planning, development, and test; phase 3: specifications, planning, development, and test