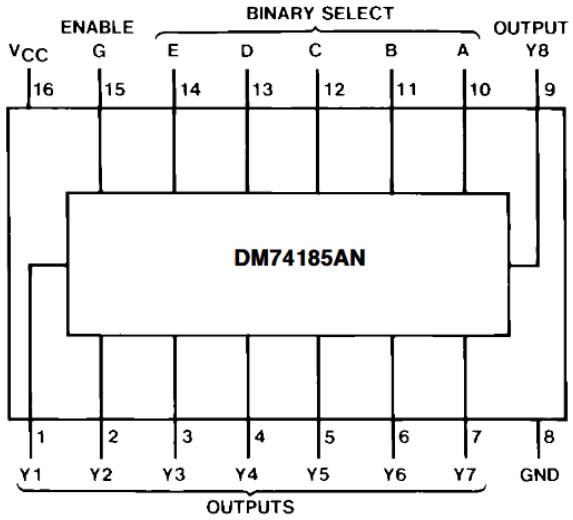
PLA2. Designing standard circuits using VHDL plans A and B

We like to invent a BCD counter later on in project P7 where the functionality of converting binary code to BCD to drive 7-segment digits is required. The idea is similar to this example from instructables but naturally, replacing all obsolete MSI (medium scale of integration) chips and wires by a CPLD or an FPGA to solve all the application in a single programmable chip.

The aim of this project is to design a typical chip, an industry standard such as the 74185A using two flat single-file approaches:

- Project location L:\CSD\P2\Bin_BCD_converter_6bit\planA\ *Bin_BCD_converter_6bit.vhd*
- Project location L:\CSD\P2\Bin_BCD_converter_6bit\planB\ *Bin_BCD_cenverter_6bit.vhd*



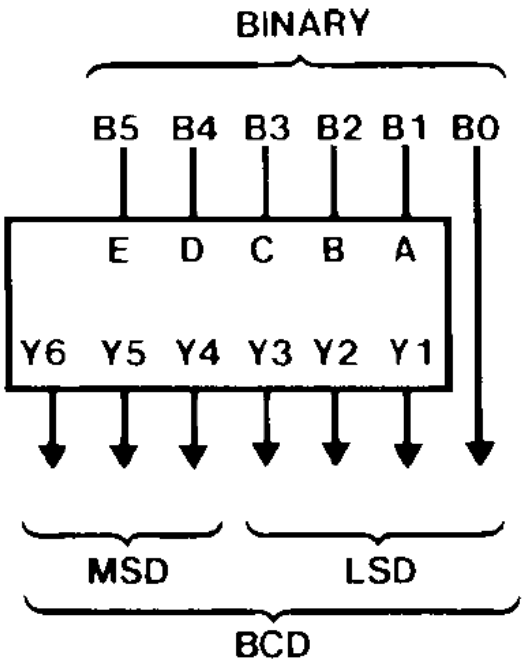


Fig. 1 Example of an obsolete MSI commercial chip 74185A. We will copy and adapt its truth table to modern VHDL language. Using a single chip is possible to implement a 6-bit binary to BCD converter. The datasheet shows that using more chips larger converters can be designed.

Let us organise how to solve these pair of projects.

1. Specifications

The chip symbol and truth table is an adaptation from the 74185A datasheet. Fig. 2 shows the main concepts related to specification section. Discuss those concepts and answer questions such:

a. What is BCD code? What is its main application? Convert a 6-bit binary number such $(52)_{10}$ to BCD. If we have to invent later on P7 a binary counter that allows counting up to 99.999.999, how many bits will be necessary?
b. Deduce the 74185A NML and NMH, and calculate limiting resistors to drive active-high the 8 LED with 10 mA bias current each in the worst-case scenario and be able in this way to represent BCD output code. Typical LED bias voltage (V_{AKQ} = 1.9 V) and typical chip from TTL logic family.
c. Deduce MAX10 NML and NMH powered at 3.3 V standard LVTTL (datasheet *table 20*), and calculate limiting resistors to drive the 2 mA/segment common-anode 7-segment displays on the DE10-Lite board (*fig. 3.17*).
d. Draw an example sketch of a timing diagram to be later at section 4 translated to a VHDL testbench file.

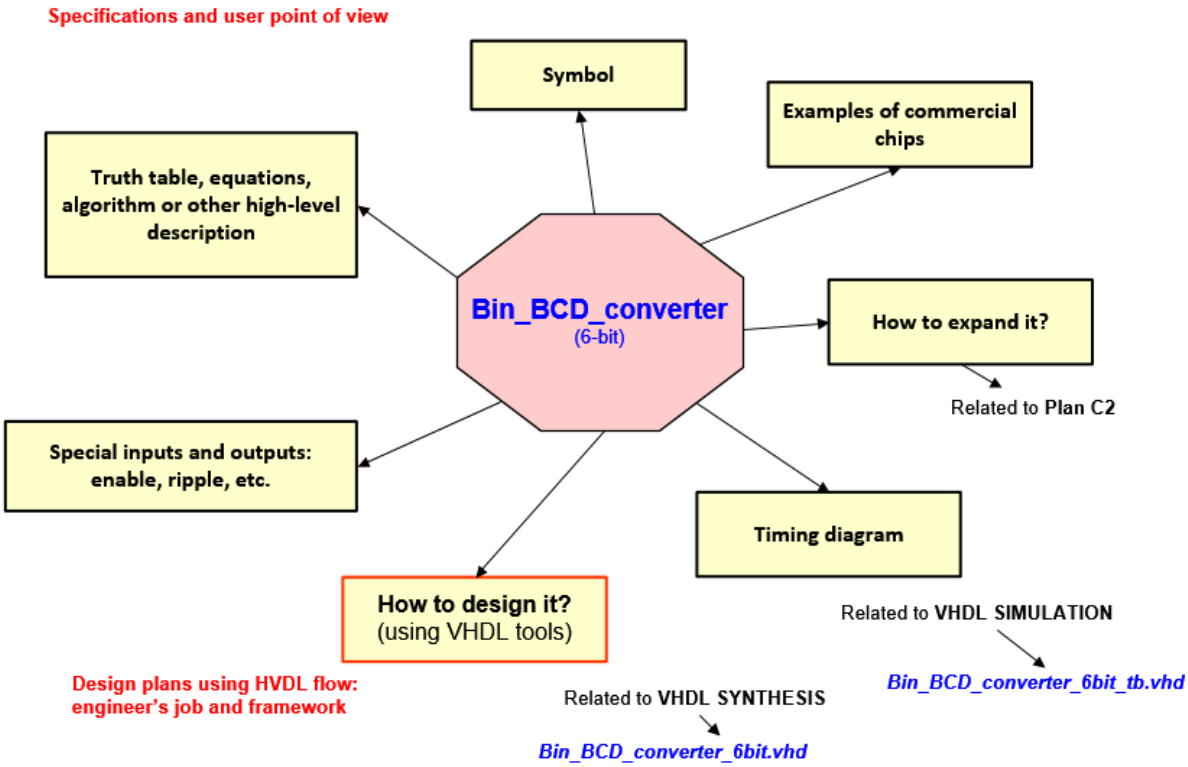


Fig. 2. Concept map to discuss combinational circuit specifications.

2. Planning

2A. Discuss and draw plan A. How to obtain a set of equations from the truth table to be translated into a VHDL architecture?

2B. Discuss and draw plan B schematics or flowcharts. How to obtain a behavioural translation of the truth table?

3. Development

Write VHDL source files, and run Quartus II for a target chip MAX10 10M50DAF484C7G.

- 3A. Plan A: synthesise a circuit and inspect the RTL and technology schematics using equations. Discuss the RTL and technology views.
- 3B. Plan B: synthesise a circuit and inspect the RTL and technology schematics using a behavioural translation of the truth table. Discuss the RTL and technology views.

4. Test and verification

Draw a VHDL testbench fixture, indicating its main parts and concepts.
Write a VHDL testbench from the timing diagram above. Start a simulation project in ModelSim.

- 4A. Plan A: Test the circuit and discuss results.
- 4B. Plan B: Test the circuit and discuss results.

5. Report and marking

Report consisting of scanned figures and handwritten discussions, organised as follows: 1 – 2A – 3A – 4A; 2B – 3B – 4B.

Section 1 on project specification is the same for both plans, thus solving and reporting it one time is all right. (2p, 0.5p each question)
Plan A sections 2A (1.5p) – 3A (1.5p)
Plan B sections 2B (1.5p) – 3B (1.5p)
Section 4 on testing designed circuits uses the same VHDL testbench for plans A and B, and naturally the same results are expected. Section 4A (1p) – 4B (1p)