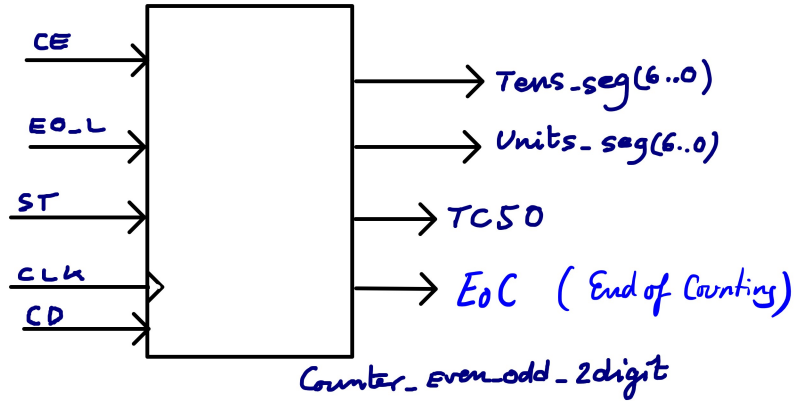
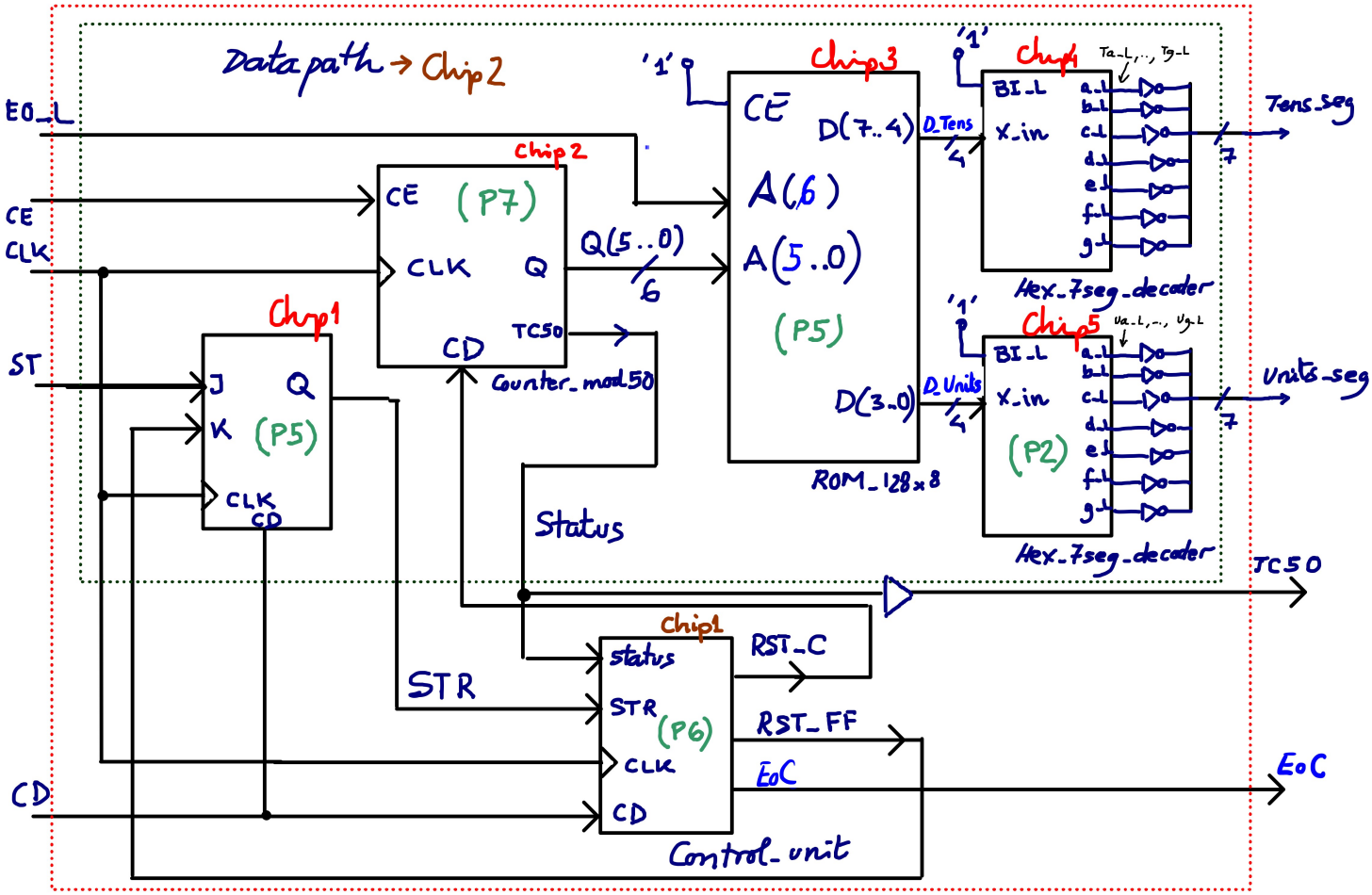
Some ideas on the design of Project 8.4

- It is an advanced system composed of datapath + control unit
- The design requires components from previous projects





status signal is '1' when CE='1' and Q is at last state

Counter_even_odd_2digit

Control signals:
- STR → Start pulse registered
- RST_C → reset counter
- RST_FF → reset flip-flop

End of operation or End of counting → EoC → ⎍⎍⎍ when stopping at the end of the counting sequence

Even or Odd numbers → EO_L = A(7) { '0' → 50 bytes (odd numbers); '1' → 50 bytes (even numbers)

Chip2 in the datapath.vhd
a) Plan Y design
b) Plan C2 using Counter_mod16 from Problems 7.2

Next idea
Solve it in P12 using a μC