Sample questions for projects P1 - P2 - P3 - P4

Analyze the circuit in the picture and deduce the output $G = f(A, B, C)$.

Select one:
- a. $G = (A' + B + C) \oplus (AB'C)$
- b. $G = ((A' + B + C) \cdot (A' + B + C') + (A' + B + C) \cdot (AB'C))'$
- c. $G = ((A + B' + C') \cdot (AB'C) + (A' + B' + C) \cdot (AB'C))'$

For a boolean function of $n$ variables $x_1, \ldots, x_n$, a sum term in which each of the $n$ variables appears once (in either its complemented or uncomplemented form) is called a maxterm.

A single maxterm $n$ gives a '0' value for just one combination of the input variables. Thus, it is possible to write the truth table of a logical function as a product of maxterms.

Select one:
- True
- False
This circuit is a hexadecimal to seven-segment decoder which has active-low outputs. The number '9' is represented. Which is the value of the output vector \([a_L, b_L, c_L, \ldots, g_L]\)?

Select one:
- a. \([1 \ 1 \ 1 \ 0 \ 0 \ 1 \ 1]\)
- b. \([1 \ 1 \ 1 \ 0 \ 0 \ 1 \ 0]\)
- c. \([0 \ 0 \ 0 \ 1 \ 1 \ 0 \ 1]\)
- d. \([0 \ 0 \ 0 \ 1 \ 1 \ 0 \ 0]\)

The picture shows the truth table resulting from the WolframAlpha numerical engine when ordered to obtain it. The function is described as: \(P = f(D1, D0, A, B)\) Thus, find the sum of minterms.

Select one:
- a. \(P = f(D1, D0, A, B) = \sum m(0, 1, 2, 6, 7, 9, 10, 12, 15)\)
- b. \(P = f(D1, D0, A, B) = \sum M(3, 4, 5, 8, 11, 13, 14)\)
- c. \(P = f(D1, D0, A, B) = \sum m(0, 1, 5, 6, 7, 10, 11, 12, 15)\)
This circuit is built using gates of the HCT (High Speed CMOS) technology that has the characteristics given below. Which statement is false?

Select one:

○ a. \( V_{IL_{\text{max}}} \) is the maximum voltage that can understand \( V_{I2} \) as a logic ‘0’

○ b. In good operation conditions, when generating a low ‘0’, \( V_{O1} \) can be higher than \( V_{OL_{\text{max}}} = 0.1 \, \text{V} \)

○ c. If \( V_{O1} \) is below the \( V_{OH_{\text{min}}} = 4.4 \, \text{V} \) the next gate input voltage \( V_{I2} \) may not understand it as a valid ‘1’.

○ d. If the NAND gate is operating correctly, when generating an output level ‘1’, \( V_{O1} \) is always above the threshold \( V_{OH_{\text{min}}} = 4.4 \, \text{V} \)
Running the EDA VHDL simulator and examining the output timing diagram we can determine the truth table of a given circuit. For instance, in the capture below, we measure that:

\[ K = f(D1, D0, A, B) = K(1100) = 0 \rightarrow M_{12} \]

\[ K(1001) = 1 \rightarrow m_9 \]

Select one:

**Answers**

- True
- False
We plan a VHDL behavioural description of a **MUX_4** as shown in the flow chart sketch below. We have found up to three possible circuits to **copy & adapt** from the digsys web belonging to MUX_4 projects. Which is preferred one?

Select one:

a. 

```vhdl
architecture truth_table of MUX_4 is
begin
Y <= Ch0 when S = "00" and E_L = '0' else
    Ch1 when S = "01" and E_L = '0' else
    Ch2 when S = "10" and E_L = '0' else
    Ch3 when S = "11" and E_L = '0' else '0';
end truth_table;
```

b. 

```vhdl
BEGIN
PROCESS (E_L, S, Ch3, Ch2, Ch1, Ch0)
BEGIN
IF E_L = '1' THEN Y <= '0'; -- disable ELSE
    IF S = "00" THEN y <= Ch0;
    ELSIF S = "01" THEN y <= Ch1;
    ELSIF S = "10" THEN y <= Ch2;
    ELSE y <= Ch3;
END IF;
END PROCESS;
END truth_table;
```

d. 

Which is the value of the limiting resistor \( R_L \) that bias the LED with \( I_D = 8mA \) in the worst case scenario?

Select one:

- **a.** \( R_L = 375 \, \Omega \)
- **b.** \( R_L = 150 \, \Omega \)
- **c.** \( R_L = 437.5 \, \Omega \)
This is a HEF4532B, a commercial encoder 8 to 3 with priority high. How many minterms have the outputs GS and Y0?

Select one:

a. GS has 8 minterms and Y0 has 6 minterms.

b. GS has 255 minterms and Y0 has 170 minterms.

c. GS has 2 minterms and Y0 has 6 minterms.
The circuit in the picture is a Comp. 8bit, a comparator of radix-2 binary numbers. Which is the output of the circuit when driven by these input vectors?

- GT ---> A > B
- EQ ---> A = B
- LT ---> A < B

Select one:
- a. GT = '1'; EQ = '0'; LT = '0'
- b. GT = '1'; EQ = '1'; LT = '0'
- c. GT = '0'; EQ = '0'; LT = '1'
- d. GT = '0'; EQ = '1'; LT = '0'

The Circuit_PQR in the picture is planned on the method of decoders, and the decoder is build internally chaining 4 components DEC_3_8. How many VHDL files will contain this hierarchical structural project?

Select one:
- a. 6 VHDL files
- b. 4 VHDL files
- c. 1 VHDL files
- d. 3 VHDL files
The circuit below is a 3-bit odd-parity generator solved using the method of multiplexers and a MUX_8. Furthermore, the MUX_8 component is build internally using MUX_2. The resulting $Y_{OP} = f(X_2, X_1, X_0)$ is faster (less propagation delay) than the circuit produced using maxterms $Y_{OP} = \prod\{0, 3, 5, 6\}$.

It detects an odd number of ones at the input $X_{(2:0)}$.

The step number 4 in this design flow, the functional simulation, allows you to measure gate delays, propagation times and the worst case scenario to deduce the maximum frequency of operation of the designed circuit.
Which is the output of the circuit?

- 0' -> Add R = A + B
- 1' -> Subtract R = A - B

Select one:
- a. \( R = "10111010"; \ Z = '0'; \ OV = '1'; \ S = '1' \)
- b. \( R = "01000101"; \ Z = '0'; \ OV = '0'; \ S = '0' \)
- c. \( R = "10110101"; \ Z = '0'; \ OV = '0'; \ S = '1' \)

The circuit in the picture is a Mult 2C, 8 bits, a binary multiplier that has a control input \( N \) to operate with radix 2 data when \( N = 0 \), and with two's complement data when \( N = 1 \). Which is the output of the circuit when driven by these input vectors?

Select one:
- a. \( P(15..0) = "1110 0111 1001 1111" \)
- b. \( P(15..0) = "1001 1111 0111 1111" \)
- c. \( P(15..0) = "0011 0110 1001 1111" \)
Timing hazards or glitches refer to unwanted transitions on the output of a combinational logic circuit. These are most commonly due to different delay paths through the gates in the circuit. In real circuitry there is always a finite propagation delay through each gate. Consider the circuit analysed below where a timing diagram shows signal transitions and hand-made annotations.

Select one:

- a. Using VHDL test benches we can measure the circuit's delay such as here (3 ns) using the functional simulation EDA tool.
- b. Using VHDL test benches we can measure the circuit's delay such as here (3 ns) using the gate-level simulation EDA tool.
- c. Using VHDL test benches we can measure the circuit's delay such as here (2 ns) using the gate-level simulation EDA tool.
- d. Using VHDL test benches we can measure the circuit's delay such as here (2 ns) using the functional simulation EDA tool.
The Adder_32 entity in the picture is based on the ripple-carry technique of 32 Adder_1bit cells, which internally are structured using 3-levels-of-logic gates as shown in the simplified macrocell. The entity is implemented in an Intel-Altera CPLD MAX7128S chip showing the characteristics in the table. Calculate the propagation delay and the maximum speed of operation.

Select one:

- a. \( t_P = 3 \text{ ns}; f_{\text{max}} = 333.3 \text{ MHz} \)
- b. \( t_P = 288 \text{ ns}; f_{\text{max}} = 3.47 \text{ MHz} \)
- c. \( t_P = 96 \text{ ns}; f_{\text{max}} = 10.4 \text{ MHz} \)