UPC. EETAC. Bachelor degree, Course 2A. Digital Circuits and Systems (CSD). Dr F. J. Robert. Grades will be available online on January 30th. Questions about the exam at office time.

Exam 2. **January 25th, 2022**

Problem 1. (2.5p)

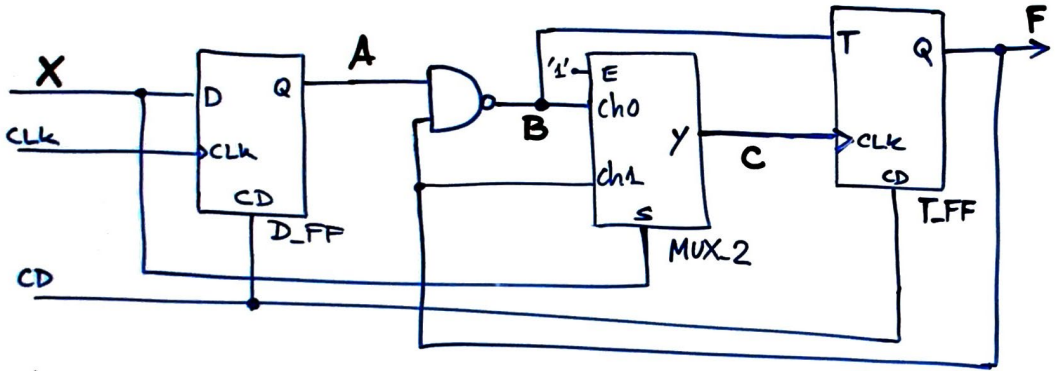
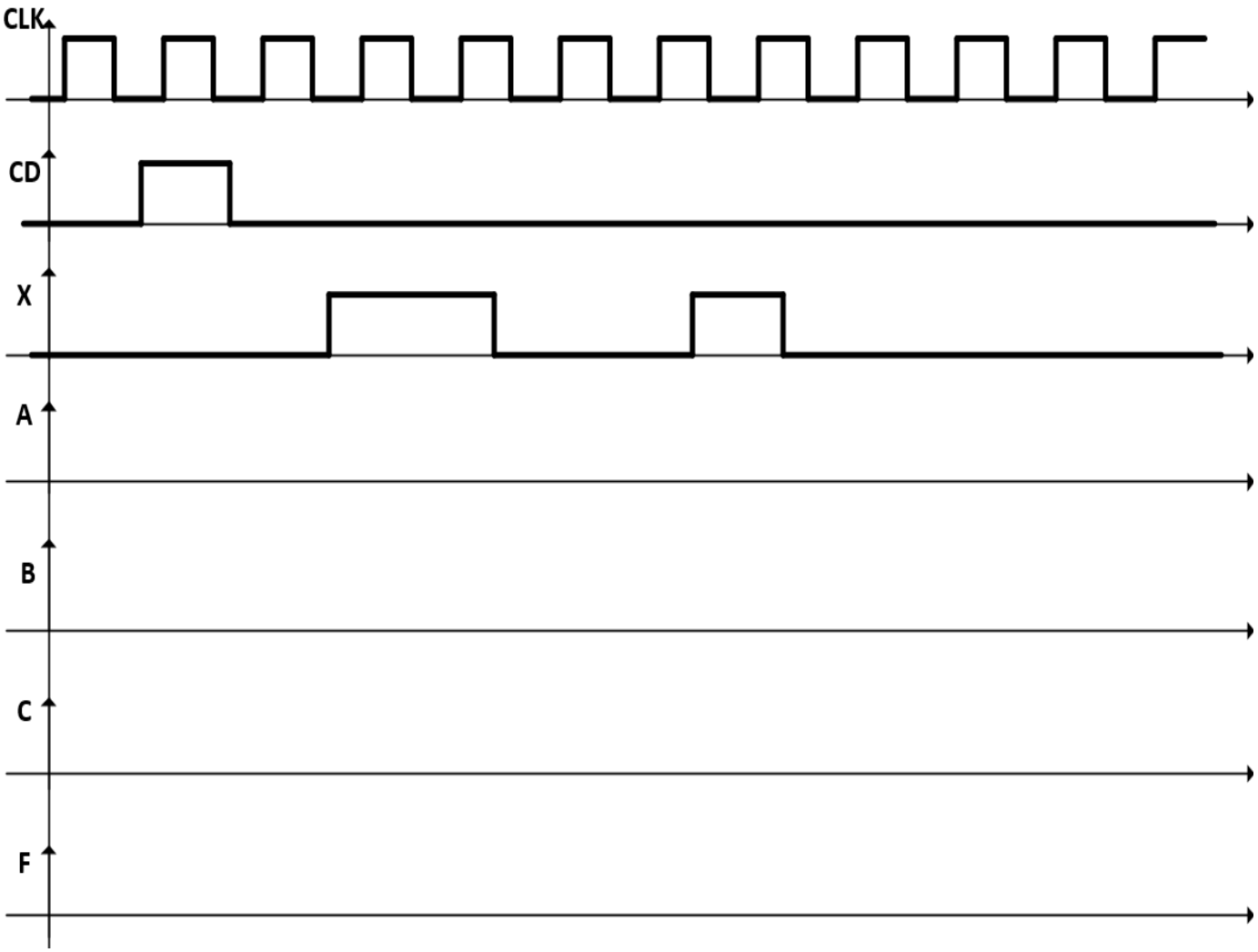


Fig. 1
Circuit based on 1-bit memory cells and combinational circuits.



1. Analyse the circuit in Fig. 1 to determine the output **F** completing the timing diagram in this sheet of paper.
2. Explain why asynchronous circuits have disadvantages respecting synchronous circuits.
3. Explain ow many VHDL files are necessary to develop and simulate the circuit using EDA tools.
4. If the propagation time of a logic gate is t_P = 2.3 ns, discuss and estimate the circuit's maximum speed.

Problem 2. (3.5p)

Design an alarm system for a refrigerator door as shown Fig. 2 using VHDL techniques and structural plan C2 for a target PLD chip. The specifications are represented in the timing diagram in Fig. 3: when the door is open for less than 20 s nothing happens, when the door is kept open for more than 20 s, the buzzer generates an alarm tone until the door is closed.

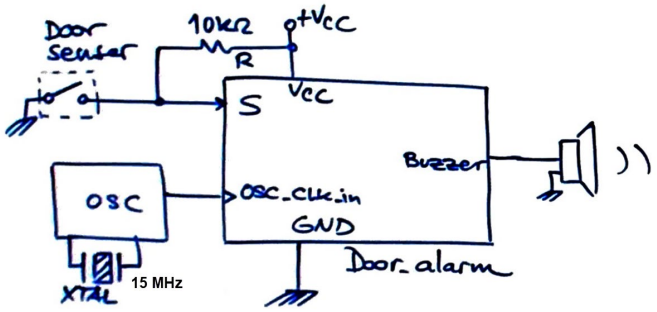


Fig. 2. Entity

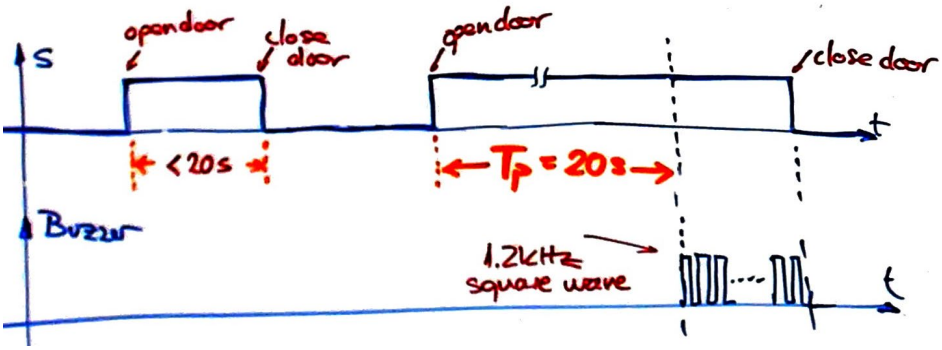


Fig. 3. Waveforms.

As shown in Fig. 4, the Chip1 FSM is controlling the Chip 2 datapath and generating an output B that is high when the alarm is on.

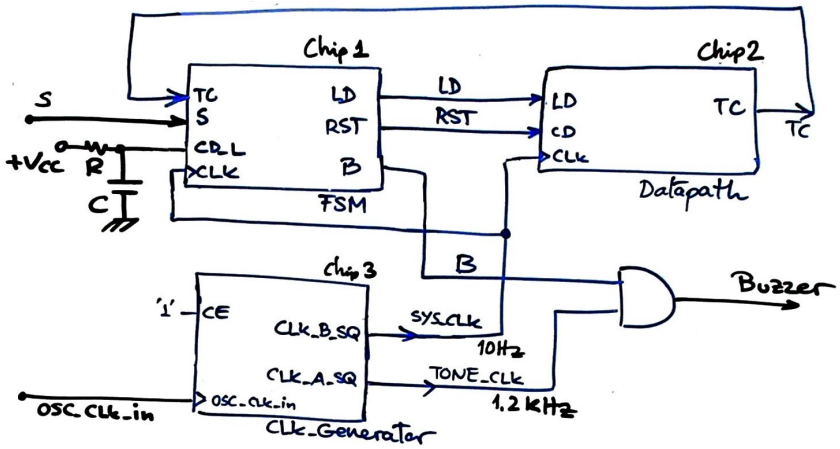


Fig. 4. Dedicated processor architecture.

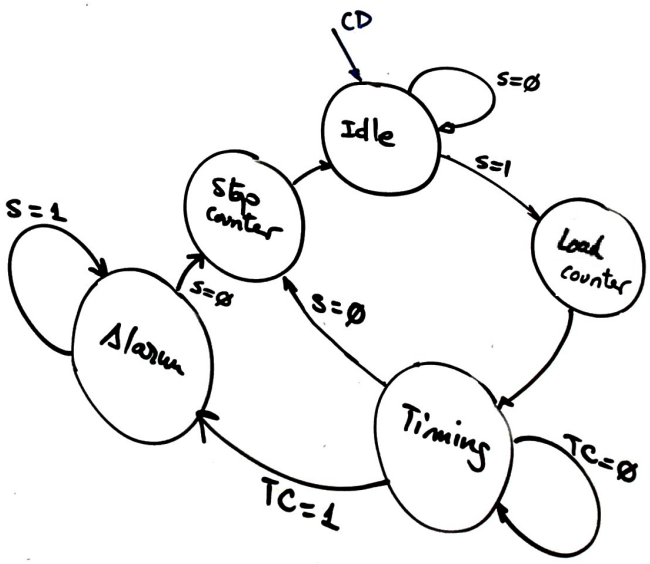
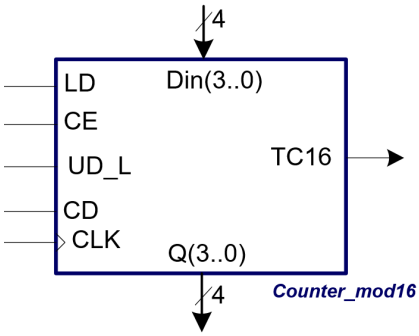


Fig. 5. State diagram proposed for Chip1 FSM showing only states and transitions.

1. Invent the *CLK_Generator* Chip3 to obtain the 1.2 kHz squared TONE_CLK and the 10 Hz SYS_CLK signals to drive the circuit from the 15 MHz crystal oscillator.
2. Complete the state diagram in Fig. 5 proposing the outputs LD, RST and B from the FSM that have to be written in parenthesis at each state.

3. Draw the Chip1 internal FSM architecture connecting all the control unit inputs and outputs. Determine the number of *D_FF* in its state register to encode internal states in one-hot.
4. Write down the Chip1 CC1 truth table and its equivalent flowchart ready for VHDL translation.
5. Invent the Chip2 datapath using *Counter_mod16* blocks (in Fig. 6) and logic circuits if necessary.



LD	CE	UD_L	Q^+	Synchronous operation after the CLK's rising edge
1	x	x	Din	Parallel load (register data)
0	0	x	Q	Do nothing (inhibit)
0	1	1	$(Q+1)_{mod16}$	Up counting in binary
0	1	0	$(Q-1)_{mod16}$	Down counting in binary

TC16 = '**1**' when CE = '1' *and* [(Q = 15 *and* UD_L = '1') *or* (Q = 0 *and* UD_L = '0')]; '0' otherwise

Fig. 6 *Counter_mod16* symbol and function table.

6. Considering the possibilities given by the datapath, propose a new state diagram for the Chip1 FSM composed of only three states.
7. Deduce the number of *D_FF* registers required for the complete project.

Problem 3. (4p)

Design the PIC18F4520 microcontroller version of the refrigerator door alarm system in Fig. 2.

1. Draw the hardware: reset (MCLR_L), 15 MHz quartz crystal oscillator, door sensor input at RC4 and buzzer output at RC3.
2. Draw and explain the hardware-software diagram supposing that the door sensor value is polled in *read_inputs()*, timing period of 20 s is generated from TRM0 interrupts, and the 1.2 kHz tone alarm signal is generated from TMR2 interrupts.
3. Organise and name RAM variables for the project. Explain how to configure port pins and interrupts in *init_system*().
4. Modify the state diagram in Fig. 5 to fit this application and explain what signals have to be generated in each state.
5. Explain how to poll the sensor value using bitwise operations in *read_inputs()*. Explain how to drive the Buzzer output pin using bitwise operations in *write_outputs().*
6. Explain the *ISR()* flowchart.
7. How to configure and program TMR0 (Fig. 7) to generate the timing period of 20 s?
8. How to configure and program TMR2 (Fig. 8) to generate the 1.2 kHz squared sound waveform?

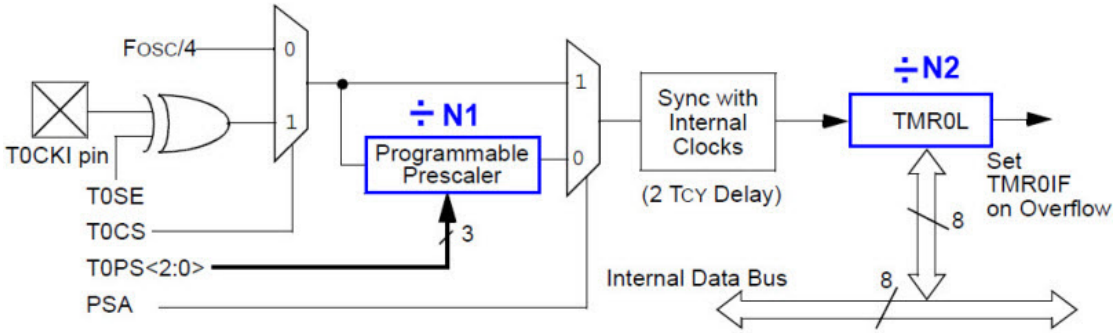


Fig. 7 TMR0 architecture for 8-bit mode.

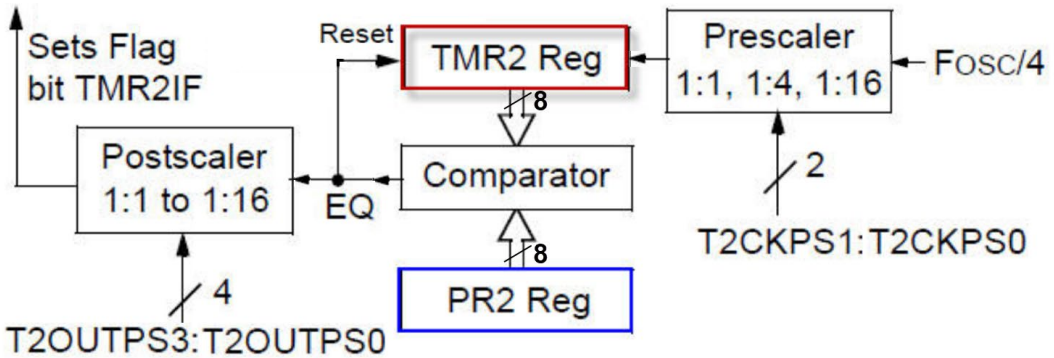


Fig. 8 TMR2 architecture.