Problem 1

(a) The state diagram has 4 states, then we need 2 D flip-flops. \( \frac{\log 4}{\log 2} \)
c) CCA truth table.

<table>
<thead>
<tr>
<th>PB</th>
<th>Current state</th>
<th>Next state</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>S1</td>
<td>S1</td>
</tr>
<tr>
<td>1</td>
<td>S1</td>
<td>S2</td>
</tr>
<tr>
<td>0</td>
<td>S2</td>
<td>S3</td>
</tr>
<tr>
<td>1</td>
<td>S2</td>
<td>S2</td>
</tr>
<tr>
<td>0</td>
<td>S3</td>
<td>S3</td>
</tr>
<tr>
<td>1</td>
<td>S3</td>
<td>S4</td>
</tr>
<tr>
<td>0</td>
<td>S4</td>
<td>S4</td>
</tr>
<tr>
<td>1</td>
<td>S4</td>
<td>S4</td>
</tr>
</tbody>
</table>

ASM Flowchart:

1. Case Current State?
   - Yes: S1
     - PB = 0?
       - Yes: NS ← S1
       - No: NS ← S2
   - No: S2
     - PB = 0?
       - Yes: NS ← S2
       - No: NS ← S3
   - S3
     - PB = 0?
       - Yes: NS ← S3
       - No: NS ← S4
   - S4
     - PB = 0?
       - Yes: NS ← S4
       - No: NS ← S2
### CC2 Truth Table

<table>
<thead>
<tr>
<th>Current State</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>0</td>
</tr>
<tr>
<td>S2</td>
<td>1</td>
</tr>
<tr>
<td>S3</td>
<td>1</td>
</tr>
<tr>
<td>S4</td>
<td>0</td>
</tr>
</tbody>
</table>

### ASM Flowchart

- **Current State**
  - S1: Z = 0
  - S2: Z = 1
  - S3: Z = 1
  - S4: Z = 0
Problem 2

a)

CLK  
CD  
CE  
UD-L  
Q  
TC14

b) Schematic of Counter - mod14

LD  
CE  
UD_L  
CD  
CLK  

"0000" 1401 chip 1

E Ch 1  cho

S  Y

Din  +4 Quad mux 2 chip 2

Din(3..φ)

LD  TC14

D13

K(3..φ)  Counter - mod16

Q(3..φ)  D_{23} = CE \cdot UD - L K_3 K_2 U_1 U_0
The multiplexer is used to select the truncating values, which are 0 and 13. These values are introduced to the input port Den (3:0) of the counter-mod16 by means of its LD input.

The counter-mod16 will include 4 D-flip-flops, because its component counter-mod16 has 16 states.

C) The signals D0 and D13 are the inputs of the combinational circuit that implements the selection input (S) of the Quad-MUX2 and the LD input of the Counter-mod16.

<table>
<thead>
<tr>
<th>D0</th>
<th>D13</th>
<th>S</th>
<th>LD</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>-</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>-</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Counts
Jumps to 0
Jumps to 13

From this truth table we obtain:

\[ S = D_{13} \]

\[ LD = D_0 + D_{13} \]

d) In this design there are 3 VHDL files involved:
Quad-MUX2.vhd, Counter-mod16.vhd and the top design Counter-mod14.vhd.

Counter-mod16 is organized using Plan Y, because it is much more practical than Plan X.