Example solutions for the problem

The idea is to generate a single pulse of Tclk duration after clicking the start button and when the programmable delay has ended.

The minimum delay will be 3 Tclk when MaxCount = 0.

The maximum delay will be (3 + 15) Tclk = 18 Tclk.

And so, to get longer delays it is necessary simply to get a longer MaxCount vector, which, at the same time implies resizing all the data path blocks but keep the same FSM control unit.

Inspecting the architecture and the state diagram we see that the additional 3 clk periods are necessary to start down-counting (subtracting) from the Chip1 W(3:0) data register once it has been preloaded with the MaxCount number.

0 ≤ MaxCount ≤ 15

Control the sequence

1. Preload with MaxCount
2. Subtract −1 \( W = W - 1 \) saved in B

a) Top circuit Delay.vhd; FSM.vhd; Datapath.vhd; Data_Reg_4bit.vhd; ALU.vhd; Quad_MUX2.vhd (assuming that all the components are solved in a single file) → 6 VHDL files

b) FSM → one hot ⇒ 50 FF; Data_reg_4bit ⇒ 42 FF ⇒ 132 FF
c) This is the timing diagram

CLK
CD
Start
Max_Count
"0111"
"0011"
Sel_B
LDB
B
'D0'
'0000'
'0011'
'Sel_OP'
'D0'
'01'
LDW
W
'0000'
'0011'
'0111'
'0100'
'0011'
'0100'
'0011'
'1111'
Z
Delay time = (3 + 7)Tclk = 10μs
Pulse
Delay = (3 + 3)Tclk
Current state
Idle
Dec
set output
Load B
Load B&N
Unknown
Dec
Dec
d) The FSM is organised in 3 blocks: SR, CC1, CC2

\[ \text{Pulse output} \]

\[ \text{Sel.B} \rightarrow \text{LD.B} \rightarrow \text{LDW} \}

}\text{internal control signals for the datapath}

\[ \text{Z} \]

\[ \text{next.state} \]

\[ \text{start} \]

\[ \text{Z is the status signal that comes from the datapath to indicate that a given operation is giving a zero result.} \]

If the FSM is coded in 'one-hot' we need \( r = 5 \) D-FF working in parallel in the state register.

e) \text{CC2 flow chart}

\[ \text{CASE} \]

\[ \text{current.state} ? \]

\[ \text{Idle} \]

\[ \text{Load.B} \]

\[ \text{Load.B&W} \]

\[ \text{Dec} \]

\[ \text{Set.output} \]

\[ \text{Sel.B} = \emptyset \]

\[ \text{LD.B} = \emptyset \]

\[ \text{Sel.OP} = \emptyset \]

\[ \text{LD.W} = \emptyset \]

\[ \text{Pulse} = \emptyset \]

... the same way, simply the truth table which generates all the control and output signals in each state.

\text{CC2: PROCESS (current.state)}

\text{BEGIN}

\text{CASE current.state IS}

\text{When Load.B =}

\text{Sel.B <= '0';}

\text{LDB <= '1';}

\text{Load.B&W <= "10";}

\text{LD.W <= '0';}

\text{Pulse <= '0';}

\text{END CASE}

\text{END PROCESS}
f) Flow chart for the CCL truth table → generate the next state to go

<table>
<thead>
<tr>
<th>start</th>
<th>z</th>
<th>current state</th>
<th>next state</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>Idle</td>
<td>Idle</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>Idle</td>
<td>Loop</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>Load B</td>
<td>Load B</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>Load BW</td>
<td>Dec</td>
</tr>
<tr>
<td>X</td>
<td>Ø</td>
<td>Dec</td>
<td>Dec</td>
</tr>
<tr>
<td>X</td>
<td>1</td>
<td>Dec</td>
<td>Set output</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>Set output</td>
<td>Idle</td>
</tr>
</tbody>
</table>

CASE

CASE current state IS

When Idle ⇒

IF (start = '1') THEN
  next_state ← Load B;
ELSE
  next_state ← Idle;
END IF;

END CASE

END PROCESS CCL;
Some test bench stimulus

CLK

CD

Start

Max_Count

Max_Count <= "0111";

CD <= '1';

Start <= '0';

Max_Count <= "0011";

Wait for 1.3 * CLK_period;

Max_Count <= "0111";

Wait for 0.5 * CLK_period;

CD <= '0';

Wait for 0.75 * CLK_period;

Start <= '1';

Wait for 2.55 * CLK_period;

Wait;

\[ \text{clk-period = 1 \mu s} \]

\[ \text{clk-process : process} \]

\[ \text{clk <= '0'}; \]

wait for clk_period / 2 ;

\[ \text{clk <= '1'}; \]

wait for clk_period / 2 ;

end process;

\[ \text{h) This section is about the design of the Data-reg-4bit as a FSM} \]

LD = \emptyset \text{ or } \text{LD = 1 and Dim = j}

LD = \emptyset \text{ or } \text{LD = 1 and Dim = i}

16 states

4 DFF

\Rightarrow \text{See example solutions in DigiSys.upc.edu}
i) The resolution of the system is related to the architecture and the technology.

In this application, the CLK frequency can be 103 MHz as maximum, and the minimum delay that can be programmed is (3 + 0) \( T_{\text{CLK}} = 29.1 \text{ ns} \)

So, the time resolution imaginary that another complete CLK period is required to detect the start button is

\[ 4 \times T_{\text{CLK}} = 38.8 \text{ ns} \]