Problem 1

a)

\[
\begin{array}{ccccccc}
S_0 & S_1 & S_2 & S_3 & S_4 & S_5 & S_6 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 & 0 & 0 & 0 \\
1 & 1 & 0 & 0 & 0 & 0 & 0 \\
1 & 1 & 1 & 0 & 0 & 0 & 0 \\
1 & 1 & 1 & 1 & 0 & 0 & 0 \\
1 & 1 & 1 & 1 & 1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\end{array}
\]

\[TC_{L0} = 1\] in \(S_9\) and up and CE = 1

or in \(S_0\) and down and CE = 1
b) FSM structure:

![FSM diagram]

There are 10 states, then if coded in one-hot it is required 10 D-FF and if coded in binary it is required 4 D-FF.

<table>
<thead>
<tr>
<th>CE</th>
<th>UD-L</th>
<th>Current-State</th>
<th>Next-State</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>S0</td>
<td>S0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>S0</td>
<td>S1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>S0</td>
<td>S9</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>S1</td>
<td>S1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>S1</td>
<td>S2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>S1</td>
<td>S0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>S2</td>
<td>S2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>S2</td>
<td>S3</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>S2</td>
<td>S1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>S3</td>
<td>S3</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>S3</td>
<td>S0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>S3</td>
<td>S2</td>
</tr>
</tbody>
</table>
d) Main VHDL Section of CC

\[ CC2 : \text{Process}(\text{current-state},\ CE) U D\cdot L \]
BEGIN
    IF ((current-state = \text{S}_0) \text{ AND } (CE = '1') \text{ AND } \text{UD-L} = 1) \text{ OR } ((\text{current-state} = \text{S}_0) \text{ AND } (CE = '1') \text{ AND } \text{UD-L} = 0) \text{ THEN,} 
    TC10 <= '1';
    ELSE 
    TC10 <= '0';
    END IF

CASE current-state xi
    WHEN \text{S}_0 \Rightarrow 
    Q <= "00000'' ;
    WHEN \text{S}_1 \Rightarrow 
    Q <= "10000'' ;
    WHEN \text{S}_2 \Rightarrow 
    Q <= "11000'' ;
    \vdots
    WHEN \text{S}_9 \Rightarrow 
    Q <= "00000'' ;
END CASE 
END PROCESS
e) The functional simulation is ideal
   In this case the maximum frequency can be \( \infty \)

\[
\begin{align*}
  f_{\text{max}} &= \frac{1}{t_{c0} + N \cdot t_{PD}} \\
  &\text{If } C2 \text{ has three levels of gates}
  \\
  f_{\text{max}} &= \frac{1}{48 \text{ ns} + 3 \times 17 \text{ ns}} = 103.09 \text{ MHz}
\end{align*}
\]