Problem 1.

Design a synchronous 5-bit Johnson counter with count enable and reversibility control signals as shown in the symbol in Fig. 1 using the FSM strategy.

a) Draw the Johnson code for 5 bits. Draw the state diagram indicating both, transitions and outputs.

b) Draw the FSM structure consisting of CC1 and CC2 and the state register. Indicate its inputs and outputs. How many D_FF will contain the state register if the internal states are coded in binary, and if they are coded in one-hot?

c) Draw the CC1 truth table and its equivalent behavioural representation in a flow chart.

d) Write the main VHDL sentences of CC2.

e) Which is the maximum frequency that can be assigned to the CLK signal when performing a functional simulation?

f) Which is the maximum frequency that can be assigned to the CLK signal when performing a gate-level simulation if the target chip is an Altera CPLD Max II EPM2210F324C3 that has the following characteristics:

<table>
<thead>
<tr>
<th>MAX II Device Features</th>
<th>EPM2210</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_pd (ns) gate</td>
<td>1.7</td>
</tr>
<tr>
<td>t_co (ns)</td>
<td>4.6</td>
</tr>
</tbody>
</table>

Problem 2.

Analyse the circuit in Fig. 2 drawing a timing diagram of the outputs Q(3..0). Indicate which may be a possible application of this circuit. How many VHDL files will be required to develop the project?

Fig. 1
Symbol of the sequential system

Fig. 2
Circuit based on data flip-flops.
Problem 3.

Fig. 3 shows the symbol of an application based on the PIC18F4520 (Fig. 4) running with an 8 MHz crystal quartz oscillator. The idea is to control the rotation speed of a direct current motor generating a 25 Hz waveform that has 2 possible selectable duty cycles: DC1 = 20% and DC2 = 80%. The 7-segment display will show the sign “-” when idle, and the numbers 1 or 2 depending on the DC selected by the switch. The button B starts and stops the waveform generation. Fig. 5 shows an idea of the state diagram.

**a)** Draw the two waveforms indicating the $T_{ON1}$, $T_{OFF1}$, $T_{ON2}$ and $T_{OFF2}$ periods of time.

**b)** Draw the schematic connecting the inputs and outputs to the PIC18F4520. Add the crystal oscillator and the MCLR_L circuits. Explain how to configure the inputs and outputs in the `init_system()`.

**c)** Explain how to connect and configure the TMR0 (Timer 0) peripheral to generate interrupts. Which are the necessary $N_1$ and $N_2$ values for the pre-scaler and the TMR0 counter to be able to generate all the required timing periods? 

\[ \text{Timing period} = \left( \frac{4}{F_{OSC}} \right) \cdot N_1 \cdot N_2 \]

**d)** Draw the hardware/software diagram indicating the required RAM variables and how the FSM is solved in software. How to implement the functions `read_inputs()`, `write_outputs()` and `ISR()`? How and where to drive the 7-segment display to show the sign “-” and the numbers “1” and “2”?

**e)** Complete the state diagram represented in Fig. 5 and deduce the truth tables for the main functions of the C code: `state_logic()` and `output_logic()`.

This is an idea of the state diagram proposed to run this application. It must be completed.