Problem 1.

Ideas on the exam solution

<table>
<thead>
<tr>
<th>Q4 Q3 Q2 Q1 Q0</th>
<th>CE UDL</th>
<th>Q(4..0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000 0010</td>
<td>0 0</td>
<td>0 0 0 0</td>
</tr>
<tr>
<td>0001 0001</td>
<td>1 1</td>
<td>(Q+1)</td>
</tr>
<tr>
<td>0100 0100</td>
<td>1 0</td>
<td>(Q-1)</td>
</tr>
<tr>
<td>1000 0001</td>
<td>0 0</td>
<td>one-hot</td>
</tr>
<tr>
<td>0000</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

CLK

CD

CE

UDL

Q

Do nothing

(Q=00001)

(Q=00010)

(Q=00100)

(Q=01000)

(Q=10000)

All the transitions are sensitive to the clk 5
(b) Diagram of state machine:

- CC2
- CC1
- State Register

Next-state logic
- r = 5 bit if coding in one-hot (5 D-FF)
- r = 3 bit if coding in binary or Gray (3 D-FF)

(d) State Transition Table:

<table>
<thead>
<tr>
<th>CE</th>
<th>UDL</th>
<th>S</th>
<th>Next State</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>S0</td>
<td>S0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>S0</td>
<td>S1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>S0</td>
<td>S0</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>S1</td>
<td>S0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>S1</td>
<td>S2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>S1</td>
<td>S0</td>
</tr>
</tbody>
</table>

Current State

<table>
<thead>
<tr>
<th>Current State</th>
<th>Q(4..0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>00000</td>
</tr>
<tr>
<td>S1</td>
<td>00010</td>
</tr>
<tr>
<td>S2</td>
<td>00100</td>
</tr>
<tr>
<td>S3</td>
<td>00100</td>
</tr>
<tr>
<td>S4</td>
<td>10000</td>
</tr>
</tbody>
</table>

(e) Flowchart:

- Switch
  - CASE S0
    - IF CE = 0
      - next state = S2
    - ELSE IF UDL = 1
      - next state = S3
  - ELSE
    - next state = S4
For instance, \( C_0 = 1 \); \( V_{DD} = 2 \)

\[ \text{clk} \]

Current state:

\[ S_1 \quad S_2 \quad S_3 \quad S_4 \]

\[ t_{co} = 4.7 \text{ns} \]

\[ t_p = 3.5 \text{ns} \]

\[ t_p \times 3 \text{ levels of gates} \]

(For instance, if the combinational circuit is solved using POS)

\[ f_{max} \leq \frac{1}{4.7 \text{ns} + 3.35 \text{ns}} \]

\[ f_{max} \leq \frac{1}{15.2 \text{ns}} = 65.78 \text{ MHz} \]

When \( CD = 1 \) \[ Q = 00000 \]

\[ Q(4:0) \]}
The basic idea is a FSM that is able to run the system generating the waveform when the user has clicked the ST button.
DC pins will be read

CLK, ST will generate interrupts

Value-Wave will be written to the pin Wave-out
Value-LED will be written to the pin LED-on

Value-Q The counter
Value-DC
CLK-Flag
ST-Flag
value-Wave
value-LED
current-state -> to hold a value
ASCII, for instance, representing the state of the FSM
The general code organisation

- Value-DC is read continuously
- Current state is fixed here depending on the inputs ST-Flag
- Value-LED, Value-Wave & are calculated here
- Value-Din is calculated here
- The counter variable is down counted at the CLK-Flag rate
- Any time the system's main code is interrupted by ST or CLK to generate the CLK-Flag or the ST-Flag variable

CLK-Flag for the counter
ST-Flag for controlling the sequence of states

3

(Value-Wave=0) (Value-LeDC=0) (ST-Flag = 0) (ST-Flag = 1) (Value-Din = Value-DC) (ON-LED = 1) (Value-Wave = 1) (Value-Wave = 0) (Value-LeDC = 1) (The counter variable Value-Q is decrement at the CLK-Flag rate)
4) Initialise an input means writing a '0' at the corresponding DDRx register.

Initialise a pin to be an output means writing a '1' at the corresponding DDRx.

- DDRA = 0b00000000 (all input DC)
- DDRB = 0b11111111 (all output PORTB)
- DDRC = 0b11111111 (all output)
- DDRD = 0b11111111 (PC7 output

↑ Input CLK
Input ST

5) **read_input**

\[ \text{Value_{DC}} = P/N/A \]

5) **write_output**

\[ \text{PORTC = Value_{Mux}} \]

\[ \text{PORTB = Value_{LED}} \]

CLK-PG = 1
### Table 1: Current State and Value Comparison

<table>
<thead>
<tr>
<th>Current State</th>
<th>Value_{RED}</th>
<th>Value_{Wave}</th>
<th>Value_{Q}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idle</td>
<td>0</td>
<td>0</td>
<td>x</td>
</tr>
<tr>
<td>Load_Ton</td>
<td>1</td>
<td>1</td>
<td>Value_{DC}</td>
</tr>
<tr>
<td>Down_Count_Ton</td>
<td>4</td>
<td>1</td>
<td>(It is decremented every interrupt, VALUE_FLAG)</td>
</tr>
<tr>
<td>Load_Count_Toff</td>
<td>1</td>
<td>0</td>
<td>700.VALUE_{DC}</td>
</tr>
<tr>
<td>Down_Count_Toff</td>
<td>1</td>
<td>0</td>
<td>(It is decremented every interrupt, VALUE_FLAG)</td>
</tr>
</tbody>
</table>