**UPC, EETAC. Bachelor Degree. 2A. Digital Circuits and Systems (CSD). Prof. F. J. Robert. Questions about the exam: Lecturer’s office hours. Grades will be available on November 13.**

**Exam 1**

**November 6, 2017**

**Problem 1.** A digital wind direction meter

We want to design a digital wind direction meter as seen in Fig. 1 based on an optoelectronic rotary encoder of 16 positions. The sensor disk, as shown in Fig. 1c is coded in Gray, which was originally used instead of binary code to prevent spurious output from electromechanical switches. In Fig. 2 you can see the complete electrical schematic. We want to have both, a 4-bit binary output and a 1-bit coded output (one-hot) to light a circle of 16 LED to display the wind direction.

![Image of wind compass and encoder](image-url)

**Fig. 1** a) Wind compass describing the sixteen principal bearings used to measure wind direction, b) the wind transducer, and c) the basics of the Gray to binary rotary encoder sensor.

![Image of electrical schematic](image-url)

**Fig. 2** Electrical schematic. The picture is showing Gray code “1001”, which is “1110” in binary and corresponds to the wind direction Nord-Nord-Est “NNE”.

1. Write the truth table of the Chip2 DEC_4_16. Write the functions Y7_L and Y14_L using maxterms.
2. Write the function B0 = f(A3, A2, A1, A0) as a sum of minterms and the B1 = f(A3, A2, A1, A0) as a product of maxterms.
3. Let’s minimise the Gray_Bin_Converter using Minilog obtaining the tables represented in Fig. 3. Obtain B2 as a sum of products and draw the equivalent logic circuit.

4. From the tables in Fig. 3, obtain the algebraic expression of B1 as a product of sums and draw the circuit using only NOR.

5. Plan and draw a hierarchical circuit using the method of decoders and the Chip2 DEC_4_16, for the functions B2 and B1 of the Chip1. How many files the VHDL project will contain?

6. Write the VHDL code for the DEC_4_16 using a structural style (gates) (not all the code but a portion sufficient to show how the VHDL entity and architecture is organised).

Problem 2.

7. Draw the symbol and the internal schematic of a 6-bit two’s complement adder/subtractor and determine the range of the operands and the result. Explain how the overflow (OV) flag works.

8. Perform the following operations in binary using the two’s complement (2C) 6-bit adder/subtractor from previous section 7). Check the result and deduce the Z and OV flags.

   a) \((+26)_{10} + (101010)_{2C}\)
   b) \((101010)_{2C} - (-21)_{10}\)
   c) \((+18)_{10} + (101110)_{2C}\)
   d) \((-31)_{10} - (010110)_{2C}\)

9. Represent the previous operations in a timing diagram and translate it (only the stimulus section) to a VHDL test bench using a constant Min_Pulse = 7.5 µs.

10. Determine the maximum speed of operation of the 6-bit 2C adder/subtractor if synthesised in a Xilinx technology Coolrunner CX2C256 CPLD that has the propagation delays shown below. Justify your calculations.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>XC2C256 CoolRunner-II CPLD Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPD1</td>
<td>Propagation delay single p-term</td>
<td>-</td>
<td>5.7</td>
<td>ns</td>
</tr>
<tr>
<td>TPD2</td>
<td>Propagation delay OR array</td>
<td>-</td>
<td>6.0</td>
<td>ns</td>
</tr>
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