Exam 1.  
April 21st, 2021

Problem 1.

(4p)

Analysis

Analyse the digital circuit in Fig. 1. This means finding the circuit’s truth table \( G = f(A, B, C) \).

![Fig. 1. Circuit to analyse. Electrical characteristics of the logic family.](image)

a) Draw your analysis plan using a concept map.
b) Find the circuit’s algebraic equation.
c) Apply Boolean algebra to simplify and obtain SoP (or PoS).
d) From SoP (or PoS), add missing variables to deduce the circuit’s truth table.
e) Calculate the timing diagram when the input signals are represented as waveforms in Fig. 2.
f) Represent logic values, voltages and noise margins for this logic family.
g) If a single gate dissipates 35 \( \mu \)W, calculate circuit power consumption when \( G \) is driving an active-high LED with \( I_{DO} = 5.5 \) mA and \( V_{AK} = 1.85 \) V. Calculate the LED’s limiting resistor.
h) How fast is the circuit performing the truth table?

Design

i) Design the circuit using maxterms.
j) Design the circuit using only NOR of 2 inputs.
k) Design the circuit using the method of multiplexers and a MUX_2.
l) Design the circuit using the method of decoders.

![Fig. 2.](image)
Problem 2.

Fig. 3 is the standard CD74AC151 chip, a commercial 8-channel digital multiplexer (MUX_8).

a) Rename inputs and outputs using our CSD style and draw its symbol and truth table.

b) Design it using our elemental block MUX_2 following plan C2 based on a hierarchy of components.

c) How many VHDL files will require your circuit?

![Fig. 3. CD74AC151 standard chip.](image)

Problem 3.

We have in mind inventing the circuit in Fig. 4 for performing simple 4-bit arithmetic and logic operations.

![Fig. 4. Symbol and operations performed by the arithmetic and logic unit (ALU_4bit).](image)

<table>
<thead>
<tr>
<th>OP</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>$A - B$ Arithmetic (4-bit signed integer in two's complement)</td>
</tr>
<tr>
<td>01</td>
<td>$A + B$ Arithmetic (4-bit signed integer in two's complement)</td>
</tr>
<tr>
<td>10</td>
<td>$A \oplus B$ Logic XOR</td>
</tr>
<tr>
<td>11</td>
<td>$(A \cdot B)'$ Logic NAND</td>
</tr>
</tbody>
</table>

Flags: $S$: sign bit; $OV$: overflow situation; $Z$: zero result.

<table>
<thead>
<tr>
<th>OP</th>
<th>A</th>
<th>B</th>
<th>R</th>
<th>S</th>
<th>OV</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>“0101”</td>
<td>“1010”</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>01</td>
<td>“1111”</td>
<td>“1001”</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>“1000”</td>
<td>“1000”</td>
<td></td>
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</tbody>
</table>

a) How long is the circuit’s truth table? How many minterms does Z flag contain?

b) Deduce some examples of the circuit’s truth table solving the four operations for the following data (12 stimulus). Express inputs and outputs in the right radix and indicate don’t care (‘x’) results when necessary.

A = “0101” B = “1010”
A = “1111” B = “1001”
A = “1000” B = “1000”

c) Propose an internal architecture for this ALU_4bit circuit based on plan C2. Use as component a 4-channel quadruple multiplexer (Quad_MUX_4) and other blocks and logic gates if necessary. Determine how many VHDL file contain your architecture.

d) Design flag indicators $S$, $OV$ and $Z$ using logic gates.

e) Invent the XOR block using only NAND.