Exam_1 solutions (2021Q1)

Problem 1

a) 

\[ V_i = V_c = V_{CC} = 5V \]

b) 

35 logic gates  \( I_{CC} = 0.025mA \)

\[ P_0 = (35 \times 0.025mA) \times 5V = 92.5 \mu W \]

e) Gate-level simulation

9 inputs  
2^9 = 512 combinations
If Min.Path = 13.5 ns
Complete test  
running time = 6.32 μs

d) 

5 levels of gates  
\( t_p = 135 \) ns  
74 million operations per second  
Circuit area

Problem 2

\[ T = f(C_D, D_0, A, B) = T M(1, 3, 6, 8, 10, 14) \]

a) 

This is a plan B that writes all the truth table  

<table>
<thead>
<tr>
<th>D</th>
<th>C_D</th>
<th>A</th>
<th>B</th>
<th>X_0</th>
<th>T</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

b) NoD  

\[ T = f(C_D, D_0, 0, B) = \sum m(0, 2, 4, 5, 7, 9, 11, 12, 13, 15) \]

This is another plan as a flowchart and subtracting tables  

<table>
<thead>
<tr>
<th>D_0</th>
<th>A</th>
<th>B</th>
<th>C_D</th>
<th>T</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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</tbody>
</table>

Decide the 10-input OR (all the elements in T)  

Circuit T
\( T = f(D, D_0, A, B) = \overline{T Y M(1, 3, 6, 8, 10, 14)} \)

c) MoM using a MUX-8

write the truth table and subdivide it into 8 sections

Circuit-T

\[ \begin{array}{cccc|c}
D & D_0 & A & B & T \\
\hline
0 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 1 & 0 \\
0 & 0 & 1 & 0 & 1 \\
0 & 0 & 1 & 1 & 0 \\
0 & 1 & 0 & 0 & 1 \\
0 & 1 & 0 & 1 & 0 \\
0 & 1 & 1 & 0 & 1 \\
0 & 1 & 1 & 1 & 0 \\
1 & 0 & 0 & 0 & 0 \\
1 & 0 & 0 & 1 & 0 \\
1 & 0 & 1 & 0 & 1 \\
1 & 0 & 1 & 1 & 0 \\
1 & 1 & 0 & 0 & 1 \\
1 & 1 & 0 & 1 & 0 \\
1 & 1 & 1 & 0 & 1 \\
1 & 1 & 1 & 1 & 0 \\
\end{array} \]
Prob 2

\[ T = f(D_1, D_0, A, B) = TM(1, 3, 6, 8, 10, 14) \]

d) MUX-16 using plan C2

e) Circuit T

All the project:

- 3 VHDL files
- 2 VHDL files
- testbench for simulation

Hierarchical architecture plan C2

Problem 3

a) Circuit's equation

\[ R = g(A, B, C) \]

\[ S = g(A, B, C) \]

b) Simplify

\[ (A' + C) = A + C \]
\[ (B + C) = B + C' \]
\[ [(B + C') + A' + BC] + (A + C)(A + C') \]
\[ (BC + A' + BC')C \]
\[ B(C + C') + A' + C \]
\[ R = BC + A'C \]

\[ \Rightarrow \text{Total simulation time} = 15 \times \text{Min. \_ Pulse} = 38.25\mu s \]

c) \[ R = BC + A'C = ABC + A'BC + A'BC + A'BC' \]

Truth table: \[ R = \Sigma m(1, 3, 7) \]
Problem 4

![ALU_4bit](image)

<table>
<thead>
<tr>
<th>OP</th>
<th>A</th>
<th>B</th>
<th>R</th>
<th>O</th>
<th>V</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>+ 00</td>
<td>(5)</td>
<td>(-6)</td>
<td>0101</td>
<td>0101</td>
<td>0101</td>
<td>X</td>
</tr>
<tr>
<td>- 01</td>
<td>(5)</td>
<td>(-6)</td>
<td>1001</td>
<td>0000</td>
<td>0000</td>
<td>X</td>
</tr>
<tr>
<td>AND</td>
<td>0101</td>
<td>0101</td>
<td>0101</td>
<td>0101</td>
<td>0101</td>
<td>X</td>
</tr>
<tr>
<td>XOR</td>
<td>1111</td>
<td>1111</td>
<td>0000</td>
<td>0000</td>
<td>0000</td>
<td>X</td>
</tr>
</tbody>
</table>

2C integers for arithmetic:

\[ A = \overline{0101} \]
\[ B = \overline{1010} \]
\[ A = \overline{1111} \]
\[ B = \overline{1001} \]
\[ A = \overline{0000} \]
\[ B = \overline{1000} \]

\[ \overline{0101} \] Out of range
\[ (+5) + 2(\overline{-6}) \]
\[ (+5) + 2(\overline{-6}) \]
\[ \overline{0101} \] Overflow flag

Truth table:

2^3 * 2^3 = 1024 combinations

Data range from \(-8 \leq A, B, R \leq 7\)

Z → Zero flag (true when \(R = 0000\) for arithmetic and logic operations)

S → Sign bit for arithmetic

S = 1' when negative

OV → Overflow flag

OV = 1 when out of range

\[ (+5) \]
\[ (+5) + 2\overline{(-6)} \]
b) ALU_4bit architecture example

Can be combined in a single Int. Add. Sub. 4bit using:
\[
\begin{align*}
A + B & = A + 2C(B) \\
A + (\neg B) & = A + 2C(\neg B)
\end{align*}
\]

Combining Int. Add. Sub. 4bit

\[
z = (x+y)(x'+y')
\]

\[
z = ((x+y)(x'+y'))'
\]

Only 3 NOR of 2 inputs