Problem 1. 2.5p
a) Obtain the logic expression of the function \( F = g(C, B, A) \) of the circuit in Fig. 1.
b) Simplify the function to obtain a PoS or SoP.
c) Express the logic function with only NOR.
d) Obtain the truth table of \( F = g(C, B, A) \) and the corresponding equation as a product of maxterms.

![Combinational circuit based on logic gates.](image1)

Fig. 1

Problem 2. 2.5p
The Fig. 2 shows a timing diagram for a functional simulation of the Selectable_comp_8bit comparator when \( N = '0' \), and so, the data is unsigned in radix 2.

![Timing diagram for the circuit represented below:](image2)

Fig. 2

a) How long is the circuit’s truth table? Write some values of the truth table for the input stimulus in Fig. 2 and other radix-2 (when \( N = '0' \)) and integer numbers (when \( N = '1' \)).
b) Represent a similar timing diagram deducing the new outputs suposing that now \( N = '1' \) and the same \( A \) and \( B \) input combinations in ‘0’ and ‘1’ represents data in integers (signed decimal in two’s complement).
c) Propose a plan C2 hierarchical internal design of the circuit in Fig. 2 based on simpler chips of the same kind. How many VHDL files will contain this project?
d) Explain how does the Comp_1bit works (symbol and truth table) and how many maxterms have their outputs LT and EQ. Why the truth table of this circuit is incomplete?

Problem 3. 2.5p
Deduce the output \( Y = f(A, B, C) \) timing diagram of the circuit in Fig. 3 when the input stimulus is applied. If Min_Pulse is 1.75 \( \mu \)s, how long does it take to run all the simulation of the stimulus represented?

![Combinational circuit and testbench stimulus.](image3)

Fig. 3
Problem 4.

The Fig. 4 shows the internal structure (a technology view) of the MC14560 classic chip.

![Fig. 4](image)

Symbol characteristics of a MC14560 chip in CMOS technology.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>VDD</th>
<th>Max</th>
<th>Unit</th>
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<td>Propagation Delay Time</td>
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<td>2100</td>
<td>ns</td>
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<tr>
<td>A or B to S</td>
<td>tPLH, tPHL</td>
<td>5.0</td>
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<table>
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<td>3.5V</td>
<td>2.75V</td>
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</table>

a) Calculate the chip’s power consumption if each gate drains 1 µA and is powered at 5.0 V. Calculate the limiting resistor for connecting LED (V_{AX} = 1.65 V, I_{LED} = 7 mA) at the chip active-high outputs.
b) Deduce the number of gate levels of each output function of the chip. Which is the longest propagation path?
c) Deduce the propagation time of a single gate in this CMOS technology. Which is the maximum speed of operation?
d) Which VHDL simulation allows us to measure propagation time delays in a given signal transition?
e) Which is the logic function of the cell F = g(A, B) represented in Fig. 4b that is used repeatedly in this design?

Problem 5.

The equation in Fig. 5 represents a truth table which is going to be solved in VHDL using the plan B (behavioural) and the plan C2 (hierarchical based on components).

![Fig. 5](image)

\[ y = f(x_3, x_2, x_1, x_0) = \prod_{4} M(0,1,3,6,8,9,10,13,14) \]

a) Solve the function using a plan B, a behavioural approach. Represent a schematic or flowchart and explain how to translate it into VHDL.
b) Solve the function Y using the method of decoders (MoD).
c) Solve the function Y using the method of multiplexers (MoM) and a MUX_4.
d) Invent a MUX_16 using components of the same kind (MUX_4 and MUX_2) and logic gates if necessary.
e) Solve the function Y using the method of multiplexers (MoM) and the MUX_16. How many VHDL files will contain this project?