Problem 1

\[ Y_{7-L} = f(E_L, X) = (E_L + X_3 + X_2 + X_1 + X_0) = M_7 \]

\[ Y_{14-L} = M_{14} = (E_L + X_3' + X_2 + X_1' + X_0) \]

The functions in this chip have 31 minterms and only one maxterm.

(2) Redraw the truth table in order to make it easier.

\[ B_0 = f(A_3, A_2, A_1, A_0) = \sum m (1, 2, 4, 7, 8, 11, 13, 14) \]

\[ m_2 = A_3' A_2' A_1 A_0' \]

AND

OR

Sum of minterms
\[ B_1 = \prod M(0, 1, 6, 7, 10, 11, 12, 13) \]

\[ \text{AND} \]

\[ \text{product of maxterms} \]

3. \( B_2 \) as a sum of products (SoP)

\[ B_2 = A_3 \cdot A_2' + A_3'A_2 \]

4. \( B_1 \) as a product of sums (PoS)

\[ B_1 = (A_3 + A_2 + A_1)(A_3 + A_2' + A_1)(A_3' + A_2 + A_1')(A_3 + A_2' + A_1') \]

\[ (x', y', z', w')'' = (x' + y' + z' + w')' \]

\[ B_1' = (A_3 + A_2 + A_1)' + (A_3' + A_2 + A_1)' + (A_3' + A_2' + A_1')' + (A_3 + A_2' + A_1')' \]

Let's check, for instance, \( A = "1010" \)

\[ B_1 = (1 + 0 + 1)' + (1' + 0' + 1)' + (1' + 0 + 1)' + (1 + 0' + 1)' \]

\[ = (0 + 0 + 1 + 0)' = 0 \quad \text{ok} \]
5. \( B_1 = \sum_4^{11} M(0, 1, 6, 7, 12, 13, 10, 11) \)

When \( E_L = 0 \), \( B_2 = \sum_4^{14} M(0, 1, 3, 2, 12, 13, 15, 4) \)

<table>
<thead>
<tr>
<th>A3</th>
<th>A2</th>
<th>A1</th>
<th>A0</th>
<th>X3</th>
<th>X2</th>
<th>X1</th>
<th>X0</th>
</tr>
</thead>
</table>

The outputs of the decoder are the minterms.

6. Because every output of the decoder is a simple minterm,

\[ Y_{10...} = (E_L + X_3 + X_2 + X_1 + X_0) \]

and so the other 15 equations.
It is like the P_Ch1

\[ Z = (R(5) + R(4) + R(3) + R(2) + R(1) + R(0))' \]
only when the \( i = 0 \rightarrow Z = i' \)

\[ 0V = C5 \oplus Cov \text{ when the carry of the two least terms is different } \rightarrow 0V = i' \]

\[ N = 6 \text{ bit } \rightarrow -2^5 \leq A, B, R \leq 2^5 - 1 \]
This is the integer range

\[ -32 \leq A, B, R \leq +31 \]

(8) a) \( +26 = 0101010 \)
\[ OP = 0 \quad B = 101010 \]
\[ \downarrow 000100 \]
\[ +4 \]
\[ 101010 \quad 26 + (-22) = +4 \]
\[ Z = 0 \]
\[ OV = 0 \]

b) \( A = -22 \)
\( B = -21 \)
\( OP = 1 \)
\[ 101010 \]
\[ +010101 \]
\[ 111111 \quad -22 - (-21) = -1 \]
\[ Z = 0 \]
\[ OV = 0 \]
\[ 10101 \rightarrow +21 \]
one way to calculate the speed of the circuit is supposing that the adder 6-bit is a flat structure of 3 level of gates

\[ \text{Buffer XOR Adder 6-bit (XOR or NOR)} \Rightarrow f_{\text{max}} < 27.8 \text{ MHz} \]