FLEX 10K

Embedded Programmable Logic Family

May 1998, ver. 3.11 Data Sheet

Features...

- The industry's first embedded programmable logic device (PLD) family, providing system integration in a single device
  - Embedded array for implementing megafunctions, such as efficient memory and specialized logic functions
  - Logic array for general logic functions
- High density
  - 10,000 to 250,000 typical gates (see Tables 1 and 2)
  - Up to 40,960 RAM bits; 2,048 bits per embedded array block (EAB), all of which can be used without reducing logic capacity
- System-level features
  - MultiVolt™ I/O interface support
  - 5.0-V tolerant input pins in FLEX® 10KA devices
  - Low power consumption (typical specification less than 0.5 mA in standby mode for most devices)
  - FLEX 10K and FLEX 10KA devices support peripheral component interconnect Special Interest Group's (PCI-SIG) ***PCI Local Bus Specification, Revision 2.1***
  - FLEX 10KA devices include pull-up clamping diode, selectable on a pin-by-pin basis for 3.3-V PCI compliance
  - Built-in JTAG boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1-1990, available without consuming any device logic

Table 1. FLEX 10K Device Features

Feature	EPF10K10 EPF10K10A	EPF10K20	EPF10K30 EPF10K30A	EPF10K40	EPF10K50 EPF10K50V
Typical gates (logic and RAM), *Note (1)*	10,000	20,000	30,000	40,000	50,000
Usable gates	7,000 to 31,000	15,000 to 63,000	22,000 to 69,000	29,000 to 93,000	36,000 to 116,000
Logic elements (LEs)	576	1,152	1,728	2,304	2,880
Logic array blocks (LABs)	72	144	216	288	360
Embedded array blocks (EABs)	3	6	6	8	10
Total RAM bits	6,144	12,288	12,288	16,384	20,480
Maximum user I/O pins	134	189	246	189	310

Table 2. FLEX 10K Device Features

Feature	EPF10K70	EPF10K100 EPF10K100A	EPF10K130V	EPF10K250A
Typical gates (logic and RAM), *Note (1)*	70,000	100,000	130,000	250,000
Usable gates	46,000 to 118,000	62,000 to 158,000	82,000 to 211,000	149,000 to 310,000
LEs	3,744	4,992	6,656	12,160
LABs	468	624	832	1,520
EABs	9	12	16	20
Total RAM bits	18,432	24,576	32,768	40,960
Maximum user I/O pins	358	406	470	470

Note to tables:

(1) For designs that require JTAG boundary-scan testing, the built-in JTAG circuitry contributes up to 31,250 additional gates.

…and More Features

- Devices are fabricated on advanced processes and operate with a 3.3- or 5.0-V supply voltage (see Table 3)
- In-circuit reconfigurability (ICR) via external Configuration EPROM, intelligent controller, or JTAG port
- ClockLock and ClockBoost options for reduced clock delay/skew and clock multiplication
- Built-in low-skew clock distribution trees
- 100% functional testing of all devices; test vectors or scan chains are not required

Table 3. Supply Voltages

Feature	FLEX 10K Devices	FLEX 10KA Devices
	EPF10K10 EPF10K20 EPF10K30 EPF10K40 EPF10K50 EPF10K70 EPF10K100	EPF10K10A EPF10K30A EPF10K50V EPF10K100A EPF10K130V EPF10K250A
Supply voltage (V_{CCINT})	5.0 V	3.3 V

- Flexible interconnect
  - FastTrack Interconnect continuous routing structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)

  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Tri-state emulation that implements internal tri-state buses
  - Up to six global clock signals and four global clear signals
- Powerful I/O pins
  - Individual tri-state output enable control for each pin
  - Open-drain option on each I/O pin
  - Programmable output slew-rate control to reduce switching noise
- Peripheral register for fast setup and clock-to-output delay
- Flexible package options
  - Available in a variety of packages with 84 to 600 pins (see Table 4)
  - Pin-compatibility with other FLEX 10K devices in the same package
- Software design support and automatic place-and-route provided by Altera's MAX+PLUS® II development system for 486- and Pentium-based PCs and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

Table 4. FLEX 10K Package Options & I/O Pin Count *Notes (1), (2)*

Device	84-Pin PLCC	144-Pin TQFP	208-Pin PQFP RQFP	240-Pin PQFP RQFP	256-Pin BGA	356-Pin BGA	403-Pin PGA	503-Pin PGA	599-Pin PGA	600-Pin BGA
EPF10K10	59	102	134							
EPF10K10A		102	134							
EPF10K20		102	147	189						
EPF10K30			147	189		246				
EPF10K30A		102	147	189	189	246				
EPF10K40			147	189						
EPF10K50				189		274	310			
EPF10K50V				189		274				
EPF10K70				189				358		
EPF10K100								406		
EPF10K100A				189		274				406
EPF10K130V									470	470
EPF10K250A									470	470

Notes:
(1) Contact Altera Customer Marketing for up-to-date information on package availability.
(2) FLEX 10K device package types include plastic J-lead chip carrier (PLCC), thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), ball-grid array (BGA), and pin-grid array (PGA) packages.

General Description

Altera's FLEX 10K devices are the industry's first embedded PLDs. Based on reconfigurable CMOS SRAM elements, the Flexible Logic Element MatriX (FLEX) architecture incorporates all features necessary to implement common gate array megafunctions. With up to 250,000 gates, the FLEX 10K family provides the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device.

FLEX 10K devices are configurable, and they are 100% tested prior to shipment. As a result, the designer is not required to generate test vectors for fault coverage purposes. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different gate array designs; FLEX 10K devices can be configured on the board for the specific functionality required.

Table 5 shows FLEX 10K performance for some common designs. All performance values shown were obtained with Synopsys DesignWare or LPM functions. No special design technique is required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

Table 5. FLEX 10K Performance

Application	Resources Used		Performance				Units
	LEs	EABs	-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	-4 Speed Grade	
16-bit loadable counter, *Note (1)*	16	0	204	166	125	95	MHz
16-bit accumulator, *Note (1)*	16	0	204	166	125	95	MHz
16-to-1 multiplexer, *Note (2)*	10	0	4.5	5.8	6.0	7.0	ns
256 × 8 RAM read cycle speed, *Note (3)*	0	1	185	118	103	84	MHz
256 × 8 RAM write cycle speed, *Note (3)*	0	1	106	86	77	63	MHz

Notes:
(1) The speed grade of this application is limited because of clock high and low specifications.
(2) This application uses combinatorial inputs and outputs.
(3) This application uses registered inputs and outputs.

The FLEX 10K architecture is similar to that of embedded gate arrays, the fastest-growing segment of the gate array market. As with standard gate arrays, embedded gate arrays implement general logic in a conventional "sea-of-gates" architecture. In addition, embedded gate arrays have dedicated die areas for implementing large, specialized functions. By embedding functions in silicon, embedded gate arrays provide reduced die area and increased speed compared to standard gate arrays. However, embedded megafunctions typically cannot be customized, limiting the designer's options. In contrast, FLEX 10K devices are programmable, providing the designer with full control over embedded megafunctions and general logic while facilitating iterative design changes during debugging.

Each FLEX 10K device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), microcontroller, wide-data-path manipulation, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array: it is used to implement general logic, such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

FLEX 10K devices are configured at system power-up with data stored in an Altera serial Configuration EPROM device or provided by a system controller. Altera offers the EPC1 and EPC1441 Configuration EPROMs, which configure FLEX 10K devices via a serial data stream. Configuration data can also be downloaded from system RAM or from Altera's BitBlaster™ serial download cable, ByteBlaster™ parallel port download cable, or ByteBlasterMV™ parallel port download cable. After a FLEX 10K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 320 ms, real-time changes can be made during system operation.

FLEX 10K devices contain an optimized interface that permits microprocessors to configure FLEX 10K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat a FLEX 10K device as memory and configure the device by writing to a virtual memory location, making it very easy for the designer to reconfigure the device.

Go to the *Configuration EPROMs for FLEX Devices Data Sheet*, *BitBlaster Serial Download Cable Data Sheet*, *ByteBlaster Parallel Port Download Cable Data Sheet*, *ByteBlasterMV Parallel Port Download Cable Data Sheet*, and *AN 59 (Configuring FLEX 10K Devices)* for more information.

FLEX 10K devices are supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including AHDL—and waveform design entry; compilation and logic synthesis; full simulation and worst-case timing analysis; and device configuration. The MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The MAX+PLUS II software interfaces easily with common gate array EDA tools for synthesis and simulation. For example, the MAX+PLUS II software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the MAX+PLUS II software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the MAX+PLUS II development system includes DesignWare functions that are optimized for the FLEX 10K architecture.

The MAX+PLUS II software runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.

Go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book for more information.

Functional Description

Each FLEX 10K device contains an embedded array to implement memory and specialized logic functions, and a logic array to implement general logic.

The embedded array consists of a series of EABs. When implementing memory functions, each EAB provides 2,048 bits, which can be used to create RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. When implementing logic, each EAB can contribute 100 to 600 gates towards complex logic functions, such as multipliers, microcontrollers, state machines, and DSP functions. EABs can be used independently, or multiple EABs can be combined to implement larger functions.

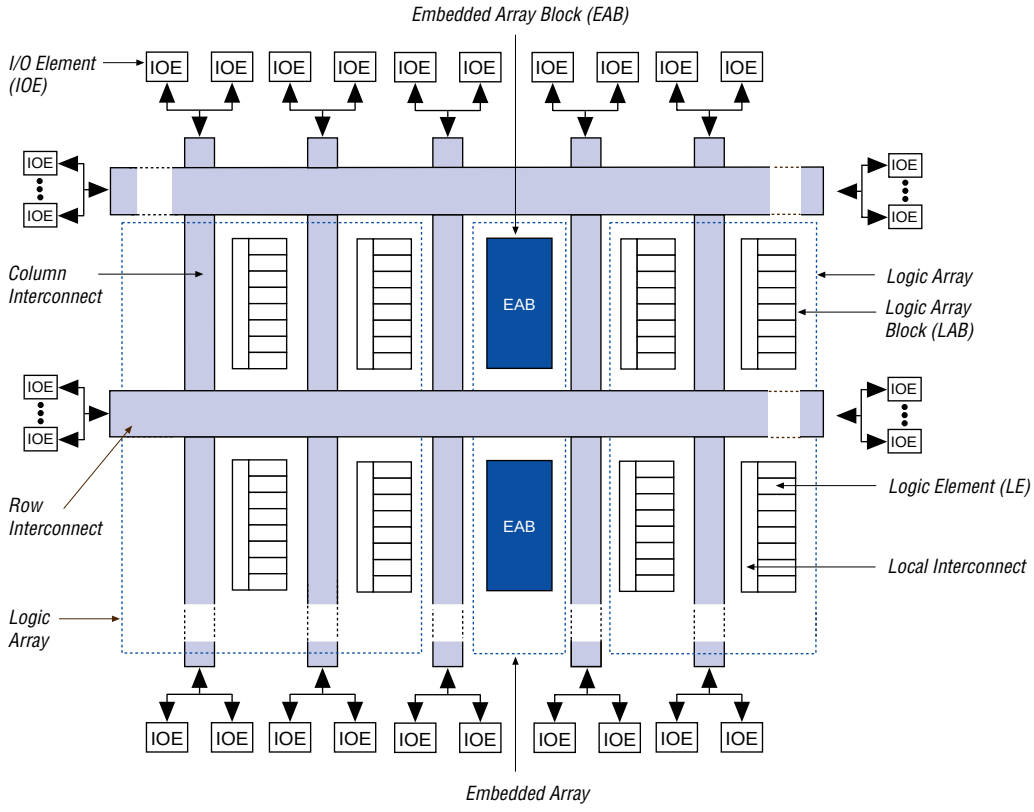
The logic array consists of logic array blocks (LABs). Each LAB contains eight LEs and a local interconnect. An LE consists of a 4-input look-up table (LUT), a programmable flipflop, and dedicated signal paths for carry and cascade functions. The eight LEs can be used to create medium-sized blocks of logic—such as 8-bit counters, address decoders, or state machines—or combined across LABs to create larger logic blocks. Each LAB represents about 96 usable gates of logic.

Signal interconnections within FLEX 10K devices and to and from device pins are provided by the FastTrack Interconnect, a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an output or input register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. As inputs, they provide setup times of as low as 3.7 ns and hold times of 0 ns; as outputs, these registers provide clock-to-output times as low as 5.3 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, tri-state buffers, and open-drain outputs.

Figure 1 shows a block diagram of the FLEX 10K architecture. Each group of LEs is combined into an LAB; LABs are arranged into rows and columns. Each row also contains a single EAB. The LABs and EABs are interconnected by the FastTrack Interconnect. IOEs are located at the end of each row and column of the FastTrack Interconnect.

Figure 1. FLEX 10K Device Block Diagram



FLEX 10K devices provide six dedicated inputs that drive the control inputs of the flipflops to ensure the efficient distribution of high-speed, low-skew (less than 1.5 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

Embedded Array Block

The EAB is a flexible block of RAM with registers on the input and output ports, and is used to implement common gate array megafunctions. The EAB is also suitable for functions such as multipliers, vector scalars, and error correction circuits, because it is large and flexible. These functions can be combined in applications such as digital filters and microcontrollers.

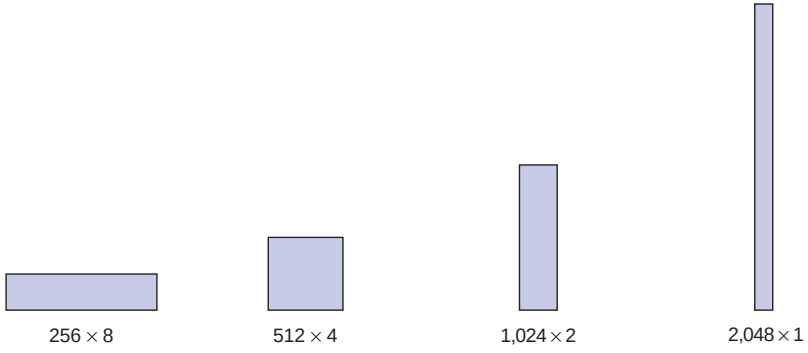
Logic functions are implemented by programming the EAB with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of EABs. The large capacity of EABs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or field-programmable gate array (FPGA) RAM blocks. For example, a single EAB can implement a 4 × 4 multiplier with eight inputs and eight outputs. Parameterized functions such as LPM functions can automatically take advantage of the EAB.

The EAB provides advantages over FPGAs, which implement on-board RAM as arrays of small, distributed RAM blocks. These FPGA RAM blocks contain delays that are less predictable as the size of the RAM increases. In addition, FPGA RAM blocks are prone to routing problems because small blocks of RAM must be connected together to make larger blocks. In contrast, EABs can be used to implement large, dedicated blocks of RAM that eliminate these timing and routing concerns.

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the EAB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. A circuit using the EAB's self-timed RAM need only meet the setup and hold time specifications of the global clock.

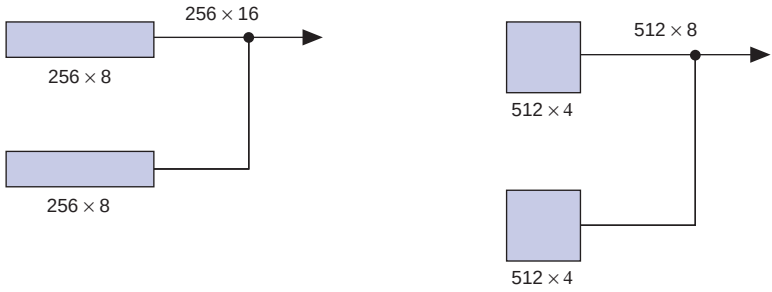
When used as RAM, each EAB can be configured in any of the following sizes: 256 × 8, 512 × 4, 1,024 × 2, or 2,048 × 1. See Figure 2.

Figure 2. EAB Memory Configurations



Larger blocks of RAM are created by combining multiple EABs. For example, two 256 × 8 RAM blocks can be combined to form a 256 × 16 RAM block; two 512 × 4 blocks of RAM can be combined to form a 512 × 8 RAM block. See Figure 3.

Figure 3. Examples of Combining EABs

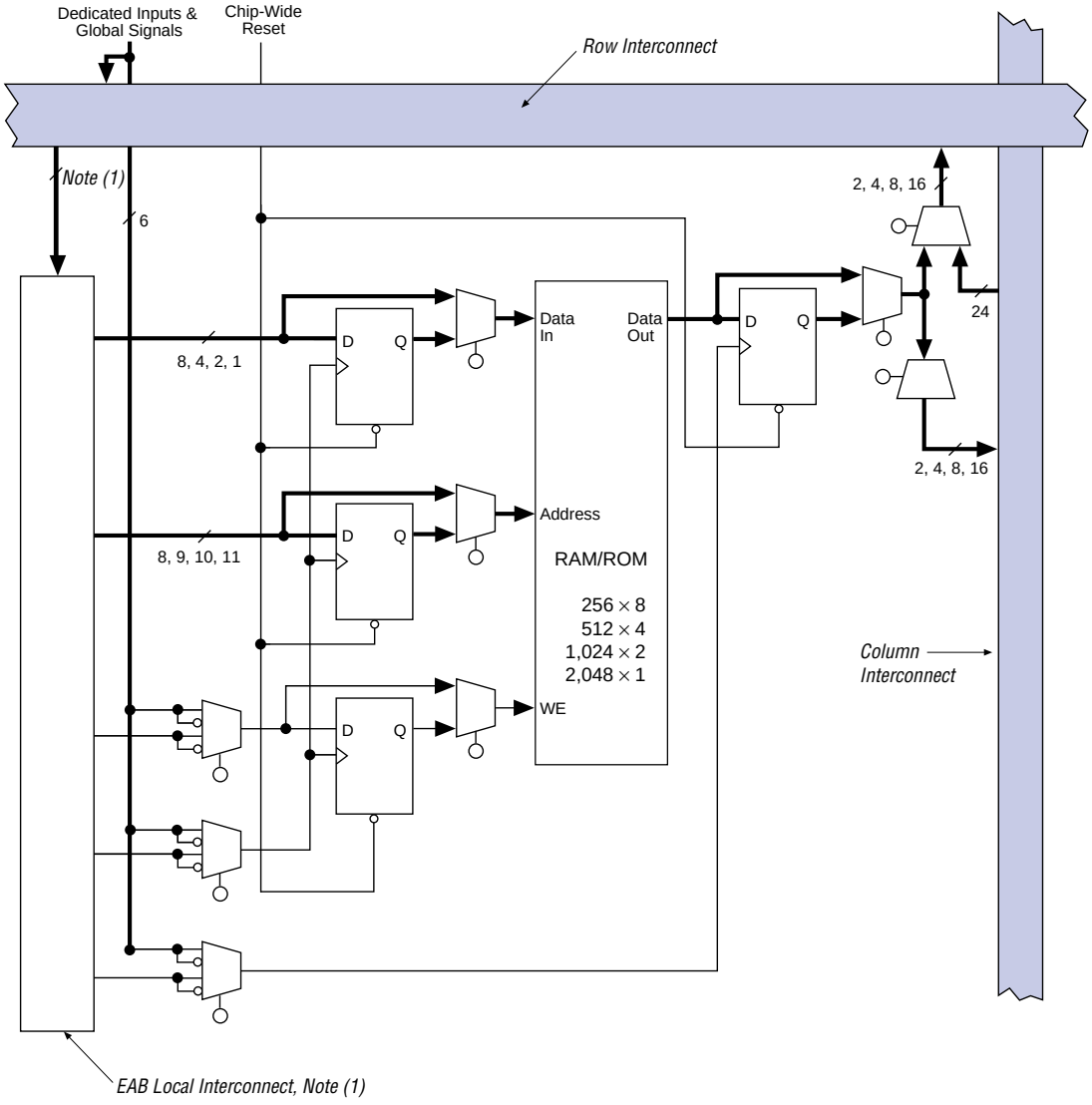


If necessary, all EABs in a device can be cascaded to form a single RAM block. EABs can be cascaded to form RAM blocks of up to 2,048 words without impacting timing. Altera's MAX+PLUS II software automatically combines EABs to meet a designer's RAM specifications.

EABs provide flexible options for driving and controlling clock signals. Different clocks can be used for the EAB inputs and outputs. Registers can be independently inserted on the data input, EAB output, or the address and WE signals. The global signals and the EAB local interconnect can drive the WE signal. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control the WE signal or the EAB clock signals.

Each EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs. See Figure 4.

Figure 4. FLEX 10K Embedded Array Block



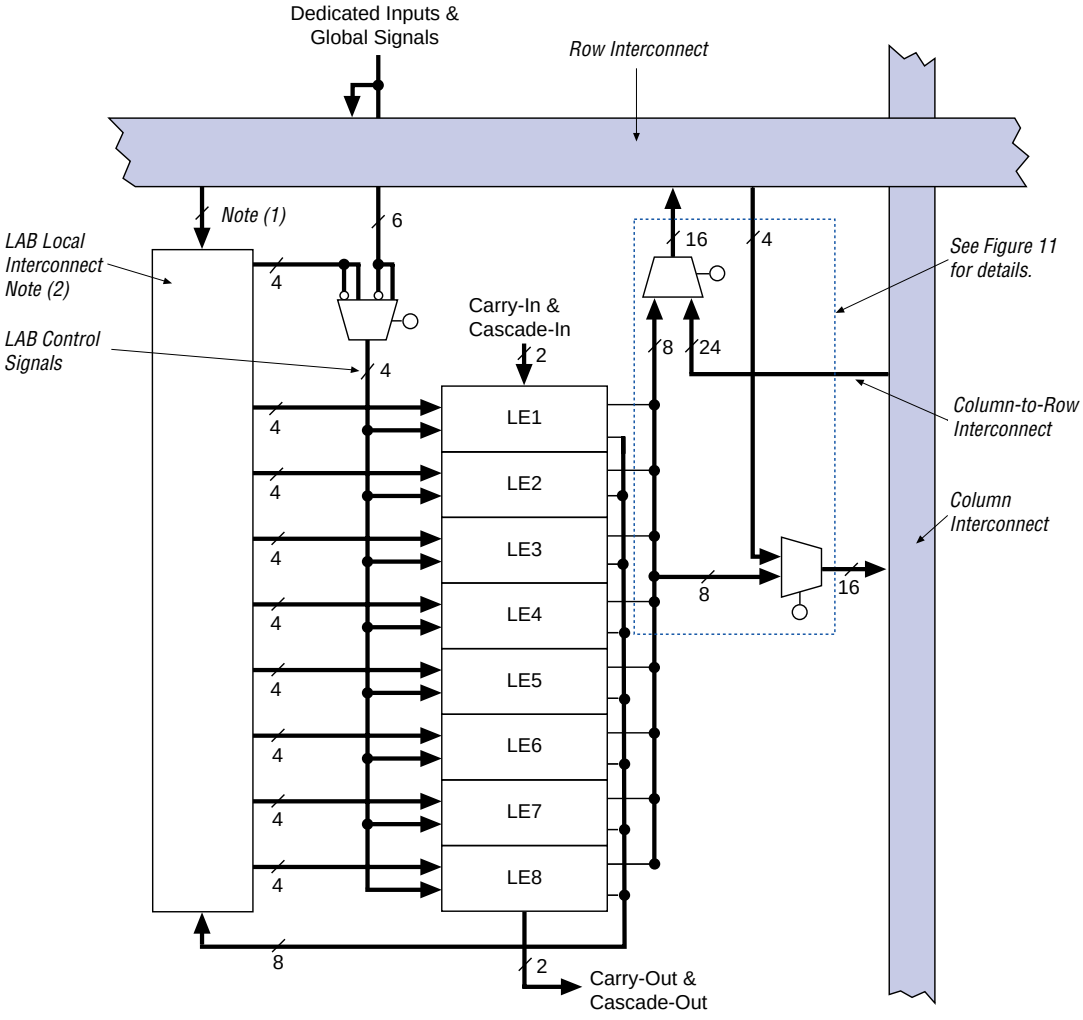
Note:

(1) EPF10K10, EPF10K10A, EPF10K20, EPF10K30, EPF10K30A, EPF10K40, EPF10K50, and EPF10K50V devices have 22 EAB local interconnect channels; EPF10K70, EPF10K100, EPF10K100A, EPF10K130V, and EPF10K250A devices have 26.

Logic Array Block

The LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10K architecture, facilitating efficient routing with optimum device utilization and high performance. See Figure 5.

Figure 5. FLEX 10K LAB



Notes:

(1) EPF10K10, EPF10K10A, EPF10K20, EPF10K30, EPF10K30A, EPF10K40, EPF10K50, and EPF10K50V devices have 22 inputs to the LAB local interconnect channel from the row; EPF10K70, EPF10K100, EPF10K100A, EPF10K130V, and EPF10K250A devices have 26.

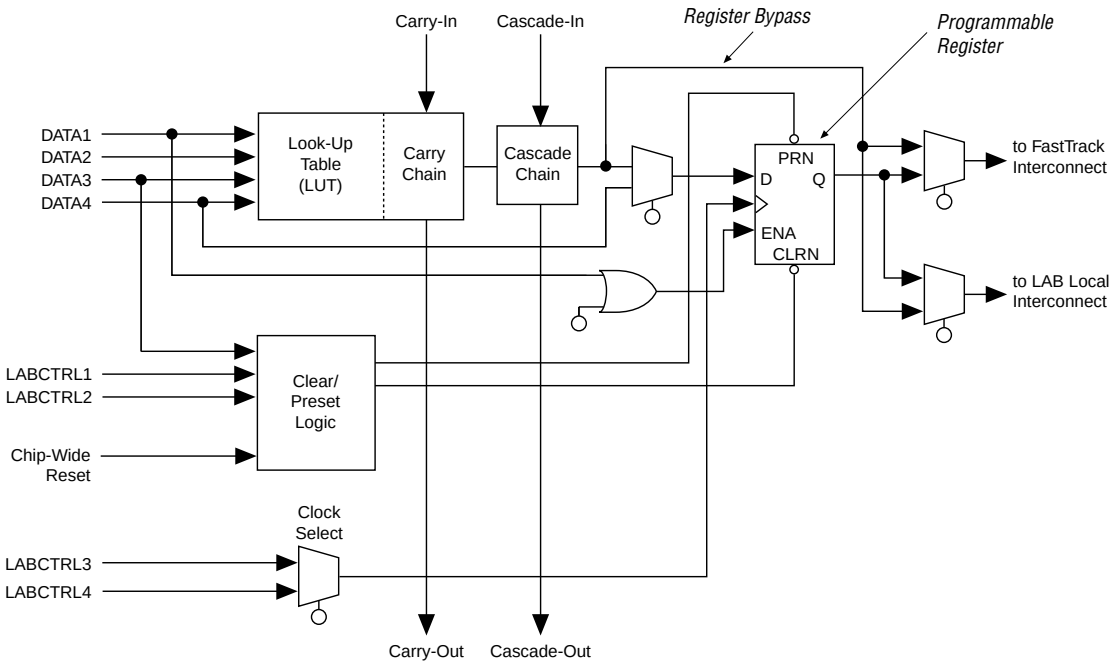
(2) EPF10K10, EPF10K10A, EPF10K20, EPF10K30, EPF10K30A, EPF10K40, EPF10K50, EPF10K50, and EPF10K50V devices have 30 LAB local interconnect channels; EPF10K70, EPF10K100, EPF10K100A, EPF10K130V, and EPF10K250A devices have 34.

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks; the other two can be used for clear/preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I/O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I/O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

Logic Element

The LE, the smallest unit of logic in the FLEX 10K architecture, has a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect. See Figure 6.

Figure 6. FLEX 10K Logic Element



The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the flipflop is bypassed and the output of the LUT drives the output of the LE.

The LE has two outputs that drive the interconnect; one drives the local interconnect and the other drives either the row or column FastTrack Interconnect. The two outputs can be controlled independently; for example, the LUT can drive one output while the register drives the other output. This feature, called register packing, can improve LE utilization because the register and the LUT can be used for unrelated functions.

The FLEX 10K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. The carry chain supports high-speed counters and adders; the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in an LAB and all LABs in the same row. Intensive use of carry and cascade chains can reduce routing flexibility. Therefore, the use of these chains should be limited to speed-critical portions of a design.

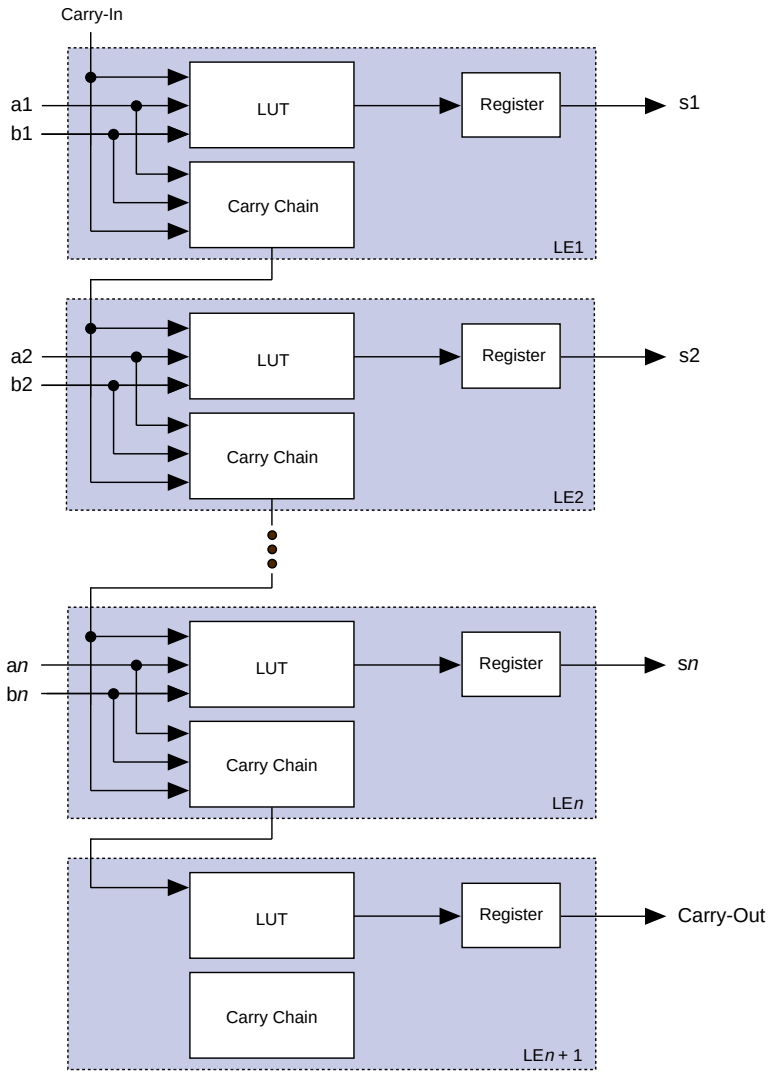
Carry Chain

The carry chain provides a very fast (as low as 0.2 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 10K architecture to implement high-speed counters, adders, and comparators of arbitrary width efficiently. Carry chain logic can be created automatically by the MAX+PLUS II Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of carry chains.

Carry chains longer than eight LEs are automatically implemented by linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a row. A carry chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB. For example, the last LE of the first LAB in a row carries to the first LE of the third LAB in the row. The carry chain does not cross the EAB at the middle of the row. For instance, in the EPF10K50 device, the carry chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB.

Figure 7 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders, but can be used for an accumulator function. Another portion of the LUT and the carry chain logic generate the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

Figure 7. Carry Chain Operation (n-bit Full Adder)



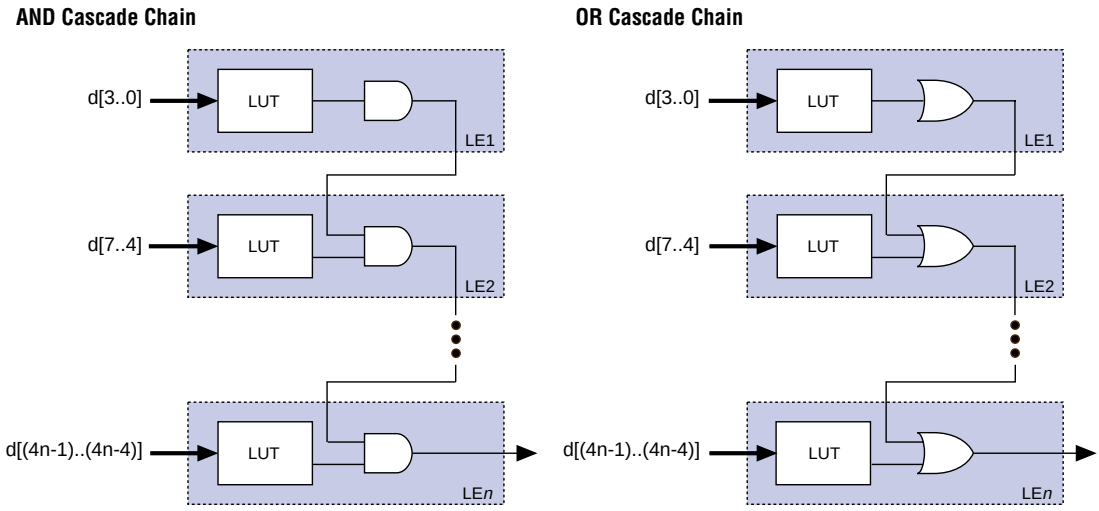
Cascade Chain

With the cascade chain, the FLEX 10K architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay as low as 0.7 ns per LE. Cascade chain logic can be created automatically by the MAX+PLUS II Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than eight bits are automatically implemented by linking several LABs together. For easier routing, a long cascade chain skips every other LAB in a row. A cascade chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB (e.g., the last LE of the first LAB in a row cascades to the first LE of the third LAB.) The cascade chain does not cross the center of the row (e.g., in the EPF10K50 device, the cascade chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB). This break is due to the EAB's placement in the middle of the row.

Figure 8 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of 4*n* variables implemented with *n* LEs. The LE delay is as low as 1.9 ns; the cascade chain delay is as low as 0.7 ns. With the cascade chain, approximately 4.2 ns is needed to decode a 16-bit address.

Figure 8. Cascade Chain Operation



LE Operating Modes

The FLEX 10K LE can operate in the following four modes:

- Normal mode
- Arithmetic mode
- Up/down counter mode
- Clearable counter mode

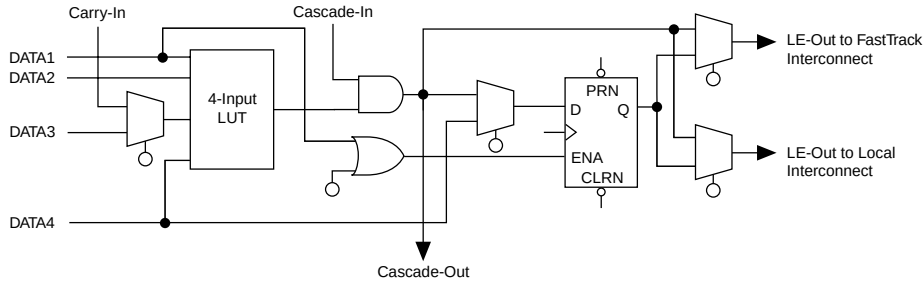
Each of these modes uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. Three inputs to the LE provide clock, clear, and preset control for the register. The MAX+PLUS II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions to use an LE operating mode for optimal performance.

The architecture provides a synchronous clock enable to the register in all four modes. The MAX+PLUS II software can set DATA1 to enable the register synchronously, providing easy implementation of fully synchronous designs.

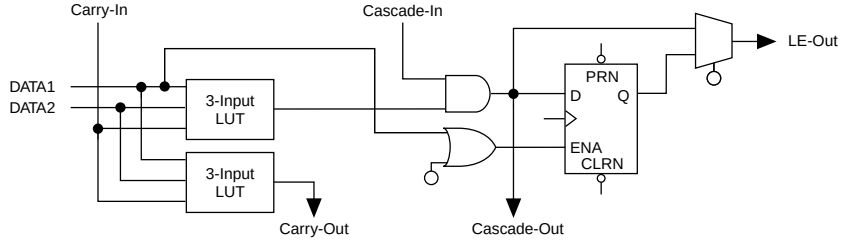
Figure 9 shows the LE operating modes.

Figure 9. FLEX 10K LE Operating Modes

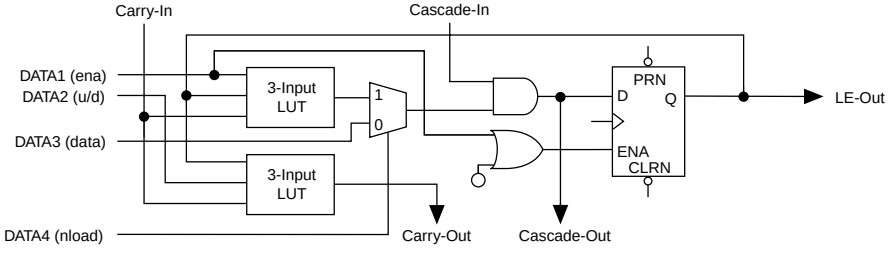
Normal Mode



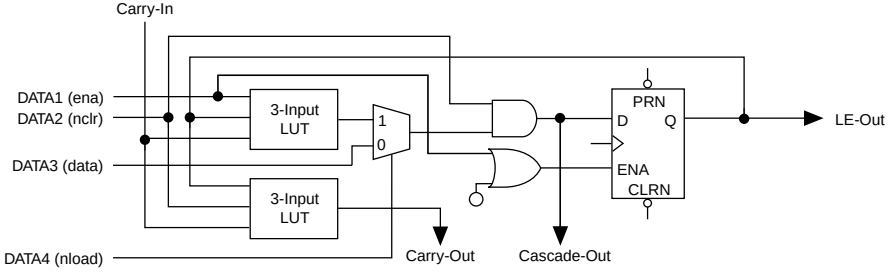
Arithmetic Mode



Up/Down Counter Mode



Clearable Counter Mode



Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a 4-input LUT. The MAX+PLUS II Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. Either the register or the LUT can be used to drive both the local interconnect and the FastTrack Interconnect at the same time.

The LUT and the register in the LE can be used independently; this feature is known as register packing. To support register packing, the LE has two outputs; one drives the local interconnect and the other drives the FastTrack Interconnect. The DATA4 signal can drive the register directly, allowing the LUT to compute a function that is independent of the registered signal; a 3-input function can be computed in the LUT, and a fourth independent signal can be registered. Alternatively, a 4-input function can be generated, and one of the inputs to this function can be used to drive the register. The register in a packed LE can still use the clock enable, clear, and preset signals in the LE. In a packed LE, the register can drive the FastTrack Interconnect while the LUT drives the local interconnect, or vice versa.

Arithmetic Mode

The arithmetic mode offers two 3-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT computes a 3-input function; the other generates a carry output. As shown in Figure 9 on page 19, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three signals: a, b, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

Up/Down Counter Mode

The up/down counter mode offers counter enable, clock enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Two 3-input LUTs are used: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals, without using the LUT resources.

Clearable Counter Mode

The clearable counter mode is similar to the up/down counter mode, but supports a synchronous clear instead of the up/down control. The clear function is substituted for the cascade-in signal in the up/down counter mode. Two 3-input LUTs are used: one generates the counter data, the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer. The output of this multiplexer is ANDed with a synchronous clear signal.

Internal Tri-State Emulation

Internal tri-state emulation provides internal tri-stating without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The MAX+PLUS II software automatically implements tri-state bus functionality with a multiplexer.

Clear & Preset Logic Control

Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE asynchronously loads signals into a register. Either LABCTRL1 or LABCTRL2 can control the asynchronous clear. Alternatively, the register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

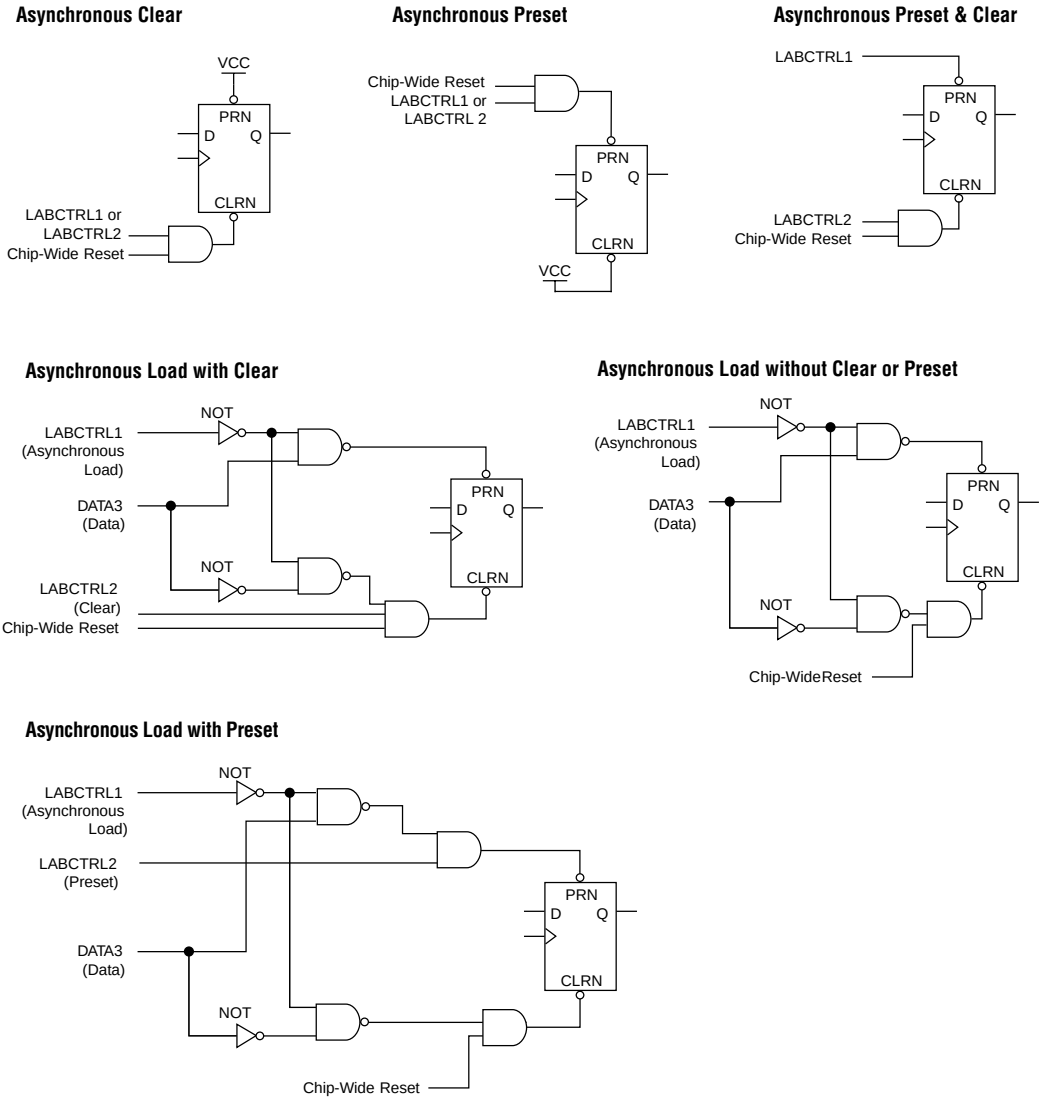
During compilation, the MAX+PLUS II Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

In addition to the six clear and preset modes, FLEX 10K devices provide a chip-wide reset pin that can reset all registers in the device. Use of this feature is set during design entry. In any of the clear and preset modes, the chip-wide reset overrides all other signals. Registers with asynchronous presets may be preset when the chip-wide reset is asserted. Inversion can be used to implement the asynchronous preset. Figure 10 shows examples of how to enter a design section for the desired functionality.

Figure 10. LE Clear & Preset Modes



Asynchronous Clear

The flipflop can be cleared by either LABCTRL1 or LABCTRL2. In this mode, the preset signal is tied to VCC to deactivate it.

Asynchronous Preset

An asynchronous preset is implemented as either an asynchronous load, or with an asynchronous clear. If DATA3 is tied to VCC, asserting LABCTRL1 asynchronously loads a one into the register. Alternatively, the MAX+PLUS II software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

Asynchronous Preset & Clear

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. DATA3 is tied to VCC, therefore, asserting LABCTRL1 asynchronously loads a one into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

Asynchronous Load with Clear

When implementing an asynchronous load in conjunction with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear; LABCTRL2 does not have to feed the preset circuits.

Asynchronous Load with Preset

When implementing an asynchronous load in conjunction with preset, the MAX+PLUS II software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 presets the register, while asserting LABCTRL1 loads the register. The MAX+PLUS II software inverts the signal that drives DATA3 to account for the inversion of the register's output.

Asynchronous Load without Preset or Clear

When implementing an asynchronous load without preset or clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

FastTrack Interconnect

In the FLEX 10K architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, which is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

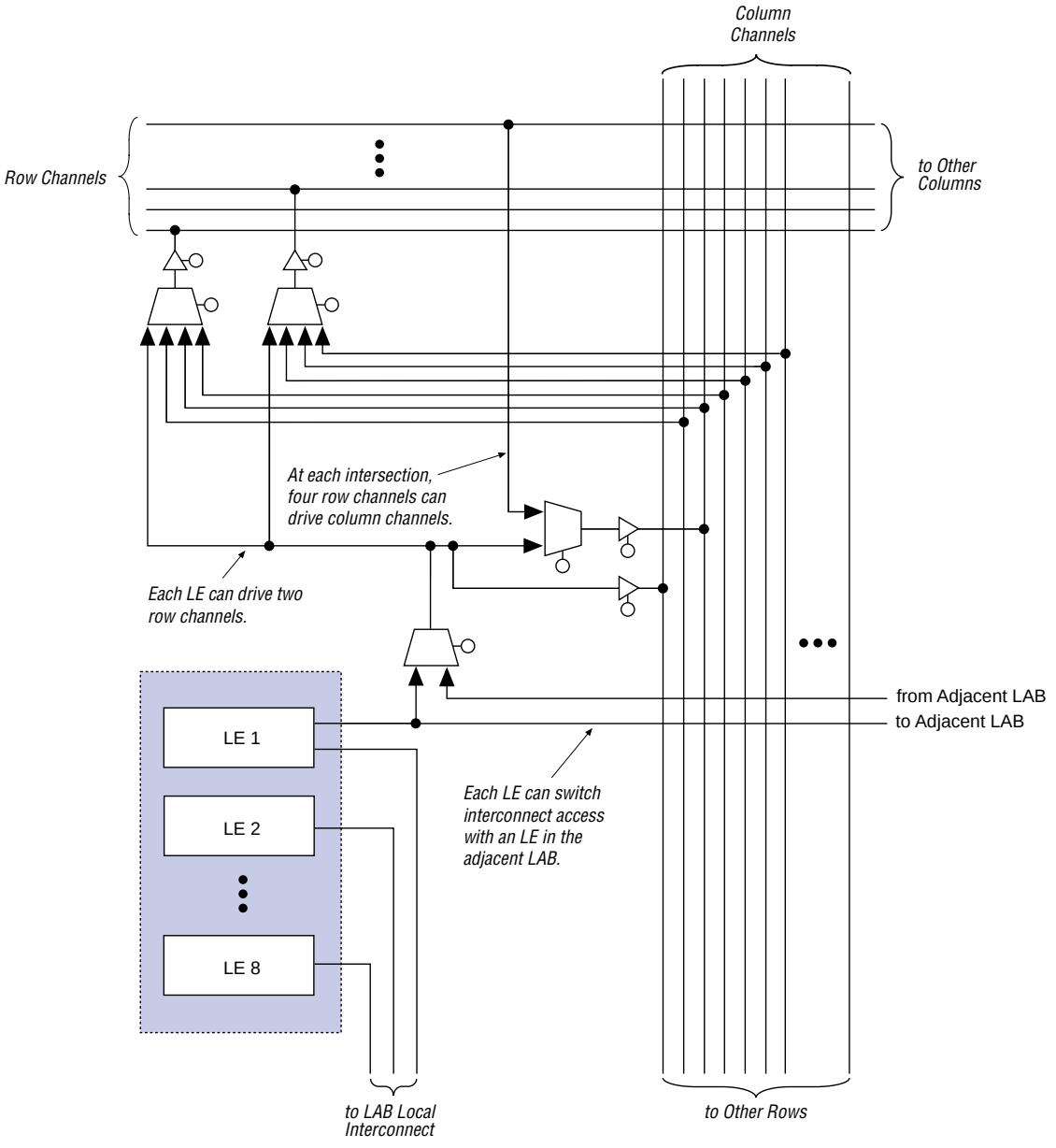
The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the device. The column interconnect routes signals between rows and can drive I/O pins.

A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in an LAB drive the row interconnect.

Each column of LABs is served by a dedicated column interconnect. The column interconnect can then drive I/O pins or another row's interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must be routed to the row interconnect before it can enter an LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, an LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This routing flexibility enables routing resources to be used more efficiently. See Figure 11.

Figure 11. LAB Connections to Row & Column Interconnect



For improved routability, the row interconnect is comprised of a combination of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in half of the row. The EAB can be driven by the half-length channels in the left half of the row and by the full-length channels. The EAB drives out to the full-length channels. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-row channel, thereby saving the other half of the channel for the other half of the row.

Table 6 summarizes the FastTrack Interconnect resources available in each FLEX 10K device.

Table 6. FLEX 10K FastTrack Interconnect Resources

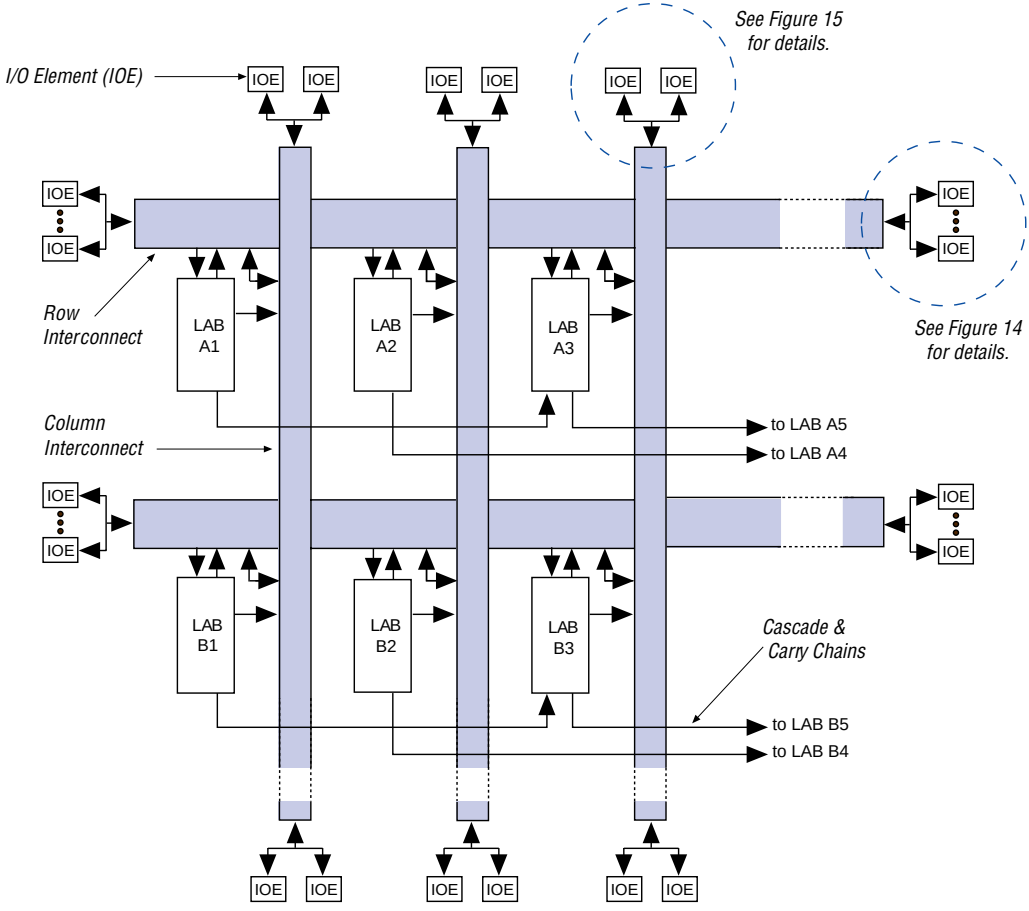
Device	Rows	Channels per Row	Columns	Channels per Column
EPF10K10 EPF10K10A	3	144	24	24
EPF10K20	6	144	24	24
EPF10K30 EPF10K30A EPF10K30E	6	216	36	24
EPF10K40	8	216	36	24
EPF10K50 EPF10K50V	10	216	36	24
EPF10K70	9	312	52	24
EPF10K100 EPF10K100A	12	312	52	24
EPF10K130V	16	312	52	32
EPF10K250A	20	456	76	40

In addition to general-purpose I/O pins, FLEX 10K devices have six dedicated input pins that provide low-skew signal distribution across the device. These six inputs can be used for global clock, clear, preset, and peripheral output enable and clock enable control signals. These signals are available as control signals for all LABs and IOEs in the device.

The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device. However, the use of dedicated inputs as data inputs can introduce additional delay into the control signal network.

Figure 12 shows the interconnection of adjacent LABs and EABs, with row, column, and local interconnects, as well as the associated cascade and carry chains. Each LAB is labeled according to its location: a letter represents the row and a number represents the column. For example, LAB B3 is in row B, column 3.

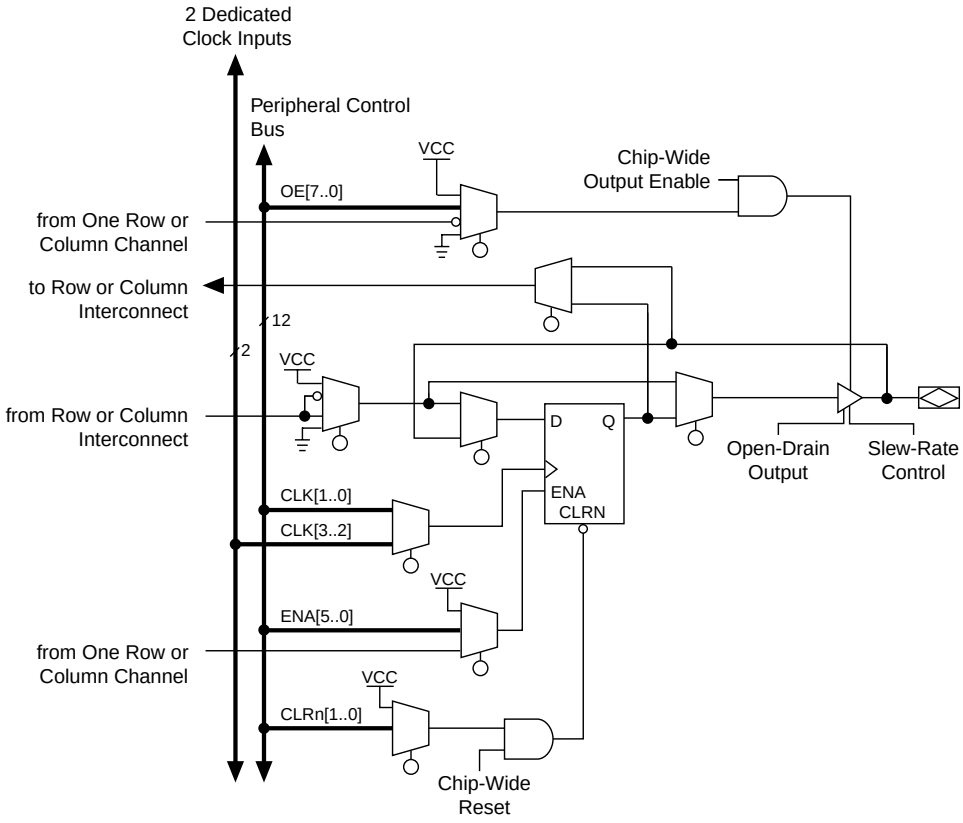
Figure 12. Interconnect Resources



I/O Element

An I/O element (IOE) contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. In some cases, using an LE register for an input register will result in a faster setup time than using an IOE register. IOEs can be used as input, output, or bidirectional pins. The MAX+PLUS II Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Figure 13 shows the IOE block diagram.

Figure 13. I/O Element



Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across devices; it provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock enable or eight output enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, an LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal will reset all IOE registers, overriding any other control signals.

Tables 7 and 8 list the sources for each peripheral control signal, and the tables show how the output enable, clock enable, clock, and clear signals share 12 peripheral control signals, and shows the rows that can drive global signals.

Table 7. Peripheral Bus Sources

Peripheral Control Signal	EPF10K10 EPF10K10A	EPF10K20	EPF10K30 EPF10K30A EPF10K30B	EPF10K40	EPF10K50 EPF10K50 EPF10K50B
OE0	Row A	Row A	Row A	Row A	Row A
OE1	Row A	Row B	Row B	Row C	Row B
OE2	Row B	Row C	Row C	Row D	Row D
OE3	Row B	Row D	Row D	Row E	Row F
OE4	Row C	Row E	Row E	Row F	Row H
OE5	Row C	Row F	Row F	Row G	Row J
CLKENA0/CLK0/GLOBAL0	Row A	Row A	Row A	Row B	Row A
CLKENA1/OE6/GLOBAL1	Row A	Row B	Row B	Row C	Row C
CLKENA2/CLR0	Row B	Row C	Row C	Row D	Row E
CLKENA3/OE7/GLOBAL2	Row B	Row D	Row D	Row E	Row G
CLKENA4/CLR1	Row C	Row E	Row E	Row F	Row I
CLKENA5/CLK1/GLOBAL3	Row C	Row F	Row F	Row H	Row J

Table 8. More Peripheral Bus Sources

Peripheral Control Signal	EPF10K70	EPF10K100 EPF10K100A EPF10K100B	EPF10K130V EPF10K130B	EPF10K250A EPF10K250B
OE0	Row A	Row A	Row C	Row E
OE1	Row B	Row C	Row E	Row G
OE2	Row D	Row E	Row G	Row I
OE3	Row I	Row L	Row N	Row P
OE4	Row G	Row I	Row K	Row M
OE5	Row H	Row K	Row M	Row O
CLKENA0/CLK0/GLOBAL0	Row E	Row F	Row H	Row J
CLKENA1/OE6/GLOBAL1	Row C	Row D	Row F	Row H
CLKENA2/CLR0	Row B	Row B	Row D	Row F
CLKENA3/OE7/GLOBAL2	Row F	Row H	Row J	Row L
CLKENA4/CLR1	Row H	Row J	Row L	Row N
CLKENA5/CLK1/GLOBAL3	Row E	Row G	Row I	Row K

Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3 in Tables 7 and 8. The internally generated signal can drive the global signal, providing the same low-skew, low-delay characteristics for an internally generated signal as for a signal driven by an input. This feature is ideal for internally generated clear or clock signals with high fan-out. When a global signal is driven by internal logic, the dedicated input pin that drives that global signal cannot be used. The dedicated input pin should be driven to a known logic state (such as ground) and not be allowed to float.

The chip-wide output enable pin is an active-low pin that can be used to tri-state all pins on the device. This option can be set in the design file. Additionally, the registers in the IOE can be reset by the chip-wide reset pin.

Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel. See Figure 14.

Figure 14. FLEX 10K Row-to-IOE Connections

The values for m and n are provided in Table 9.

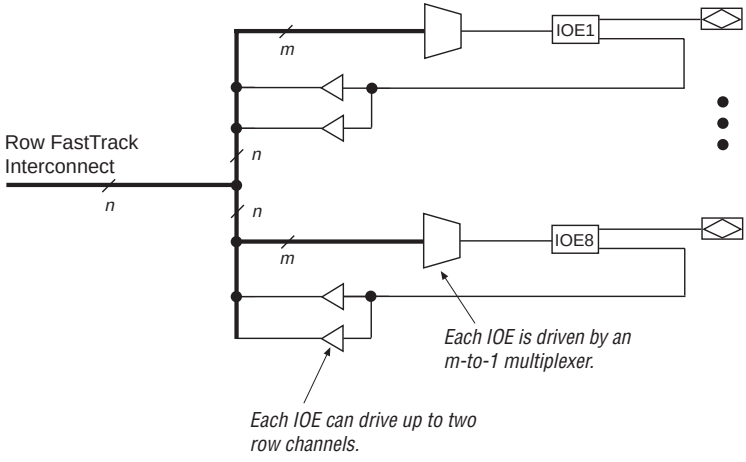


Table 9 lists the FLEX 10K row-to-IOE interconnect resources.

Table 9. FLEX 10K Row-to-IOE Interconnect Resources

Device	Channels per Row *(n)*	Row Channels per Pin *(m)*
EPF10K10 EPF10K10A	144	18
EPF10K20	144	18
EPF10K30 EPF10K30A	216	27
EPF10K40	216	27
EPF10K50 EPF10K50V	216	27
EPF10K70	312	39
EPF10K100 EPF10K100A	312	39
EPF10K130V	312	39
EPF10K250A	456	57

Column-to-IOE Connections

When an IOE is used as an input, it can drive up to two separate column channels. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the column channels. Two IOEs connect to each side of the column channels. Each IOE can be driven by column channels via a multiplexer. The set of column channels that each IOE can access is different for each IOE. See Figure 15.

Figure 15. FLEX 10K Column-to-IOE Connections

The values for m and n are provided in Table 10.

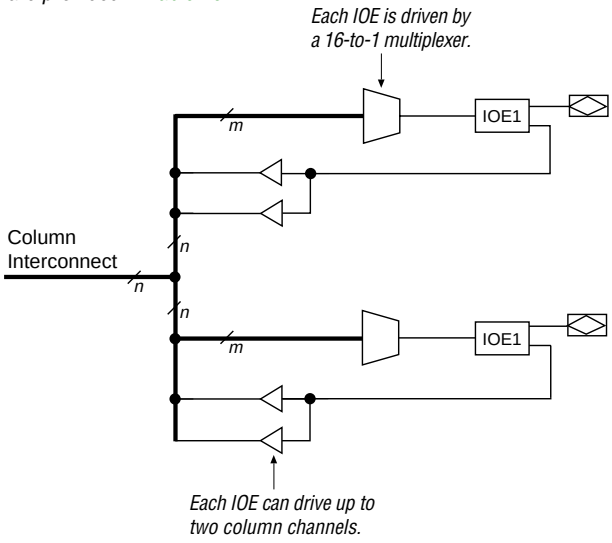


Table 10 lists the FLEX 10K column-to-IOE interconnect resources.

Table 10. FLEX 10K Column-to-IOE Interconnect Resources

Device	Channels per Column *(n)*	Column Channel per Pin *(m)*
EPF10K10 EPF10K10A	24	16
EPF10K20	24	16
EPF10K30 EPF10K30A	24	16
EPF10K40	24	16
EPF10K50 EPF10K50V	24	16
EPF10K70	24	16
EPF10K100 EPF10K100A	24	16
EPF10K130V	32	24
EPF10K250A	40	32

ClockLock & ClockBoost Features

To support high-speed designs, selected FLEX 10K devices offer optional ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL) that is used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by resource sharing within the device. ClockBoost allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, the ClockLock and ClockBoost features provide significant improvements in system performance and bandwidth.

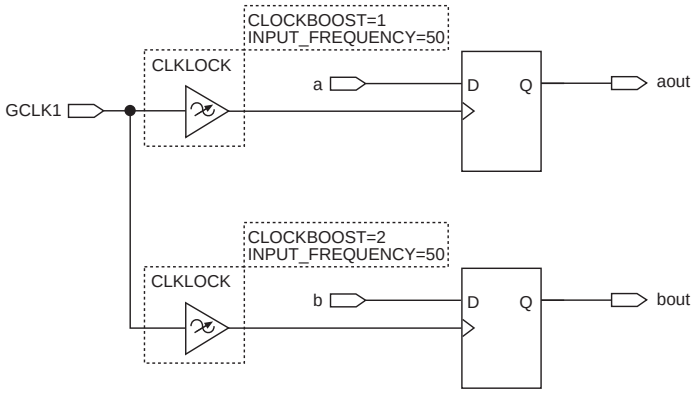
The ClockLock and ClockBoost features in FLEX 10K devices are enabled through the MAX+PLUS II software. External devices are not required to use these features. The output of the ClockLock and ClockBoost circuits is not available at any of the device pins.

The ClockLock and ClockBoost circuitry locks onto the rising edge of the incoming clock. The circuit output can only drive the clock inputs of registers; the generated clock cannot be gated or inverted.

The dedicated clock pin (GCLK1) supplies the clock to the ClockLock and ClockBoost circuitry. When the dedicated clock pin is driving the ClockLock or ClockBoost circuitry, it cannot drive elsewhere in the device.

In designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to GCLK1. With the MAX+PLUS II software, GCLK1 can feed both the ClockLock and ClockBoost circuitry in the FLEX 10K device. However, when both circuits are used, the other clock pin (GCLK0) cannot be used. Figure 16 shows a block diagram of how to enable both the ClockLock and ClockBoost circuits in the MAX+PLUS II software. The example shown is a schematic, but a similar approach applies for designs created in AHDL, VHDL, and Verilog HDL. When the ClockLock and ClockBoost circuits are used simultaneously, the input frequency parameter must be the same for both circuits. In Figure 16, the input frequency must meet the requirements specified when the ClockBoost multiplication factor is two.

Figure 16. Enabling ClockLock & ClockBoost in the Same Design



To use both the ClockLock and ClockBoost circuits in the same design, designers must use Revision C EPF10K100GC503-3DX devices and the MAX+PLUS II software, version 7.2 or higher. The revision is identified by the first digit of the date code stamped on top of the device (e.g., date code C9715 identifies a Revision C device).

For more information on using the ClockLock and ClockBoost features, see the *Clock Management with ClockLock and ClockBoost Features White Paper*, which is available from Altera Literature Services.

Output Configuration

This section discusses PCI clamping diodes, slew-rate control, open-drain output option, and MultiVolt I/O interface for the FLEX 10K devices.

PCI Clamping Diodes

FLEX 10KE (including EPF10K100B) devices have a pull-up clamping diode on every I/O, dedicated input, and dedicated clock pin. PCI clamping diodes clamp the signal to the V_{CCIO} value and are required for 3.3-V PCI compliance. Clamping diodes can also be used to limit overshoot in other systems.

Clamping diodes are controlled on a pin-by-pin basis via a logic option in the MAX+PLUS II software. When V_{CCIO} is 3.3 V, a pin which has the clamping diode turned on can be driven by a 2.5-V or 3.3-V signal, but not a 5.0-V signal. When V_{CCIO} is 2.5 V, a pin which has the clamping diode turned on can be driven by a 2.5-V signal, but not a 3.3-V or 5.0-V signal. However, a clamping diode can be turned on for a subset of pins, which would allow a device to bridge between a 3.3-V PCI bus and a 5.0-V device.

Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a maximum delay of approximately 2.9 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a device-wide basis. The slow slew rate setting affects only the falling edge of the output. Each pin can also be specified as open-drain on a pin-by-pin basis. Additionally, the MAX+PLUS II software can automatically convert tri-state buffers with grounded data inputs to open-drain pins.

Open-Drain Output Option

FLEX 10K devices provide an optional open-drain (electrically equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Open-drain output pins on FLEX10K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state, never high. Therefore, a connection will not exist between the 3.3-V and 5.0-V power supplies. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

MultiVolt I/O Interface

The FLEX 10K device architecture supports the MultiVolt I/O interface feature, which allows FLEX 10K, and FLEX 10KA, and FLEX 10KE devices to interface with systems of differing supply voltages. These devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

Table 11 describes the FLEX 10K device supply voltages and MultiVolt I/O support levels.

Table 11. Supply Voltages & MultiVolt I/O Support Levels

Device Family	Supply Voltage (V)		MultiVolt I/O Support Levels (V)	
	V_{CCINT}	V_{CCIO}	Input	Output
FLEX 10K	5.0	5.0	3.3 or 5.0	5.0
	5.0	3.3	3.3 or 5.0	3.3 or 5.0
EPF10K50V	3.3	3.3	3.3 or 5.0	3.3 or 5.0
EPF10K130V	3.3	3.3	3.3 or 5.0	3.3 or 5.0
FLEX 10KA	3.3	3.3	2.5, 3.3, or 5.0	3.3 or 5.0
	3.3	2.5	2.5, 3.3, or 5.0	2.5
FLEX 10KE (including the EPF10K100B device)	2.5	3.3	2.5, 3.3, or 5.0	3.3 or 5.0
	2.5	2.5	2.5, 3.3, or 5.0	2.5

IEEE 1149.1 (JTAG) Boundary-Scan Support

All FLEX 10K devices provide JTAG BST circuitry that comply with the IEEE Std. 1149.1-1990 specification. All FLEX 10K devices can also be configured using the JTAG pins through the BitBlaster serial download cable, ByteBlaster parallel port download cable, ByteBlasterMV parallel port download cable, or via hardware that uses the Jam™ programming and test language. JTAG BST can be performed before or after configuration, but not during configuration. FLEX 10K devices support the JTAG instructions shown in Table 12.

Table 12. FLEX 10K JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.
UESCODE	Selects the user electronic signature (UESCODE) register and places it between the TDI and TDO pins, allowing the UESCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	These instructions are used when configuring a FLEX 10K device via JTAG ports with a BitBlaster, ByteBlaster, or ByteBlasterMV download cable, or using a Jam File (**.jam**) via an embedded processor.

For more information on JTAG operation, see *Application Note 39 (JTAG Boundary-Scan Testing in Altera Devices)*. For more information on the BitBlaster, ByteBlaster, or ByteBlasterMV download cables, go to the *BitBlaster Serial Download Cable Data Sheet*, *ByteBlaster Parallel Port Download Cable Data Sheet*, and *ByteBlasterMV Parallel Port Download Cable Data Sheet* in this data book. For information on the Jam language, refer to the *Jam Programming and Test Language Specification*.

Figure 17 shows the timing requirements for the JTAG signals.

Figure 17. JTAG Waveforms

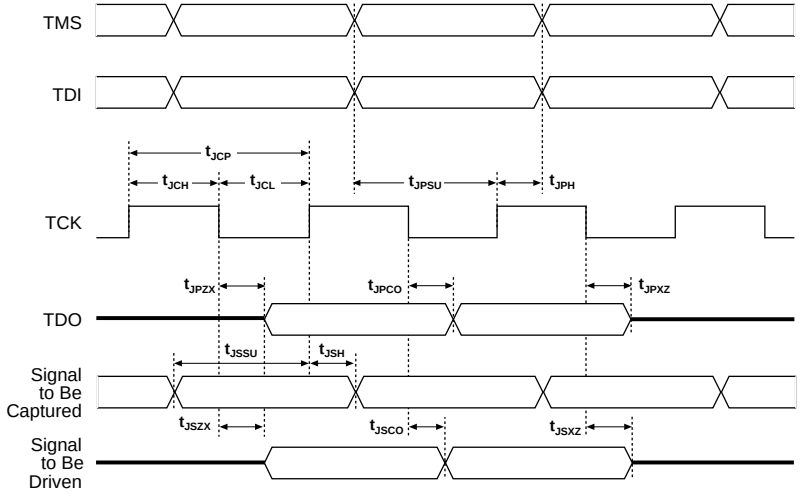


Table 13 shows the timing parameters and values for FLEX 10K devices.

Table 13. JTAG Timing Parameters & Values

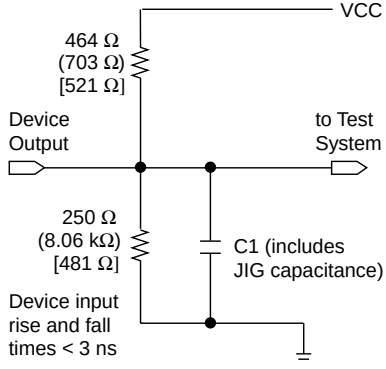
Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high-impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

Generic Testing

Each FLEX 10K device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% yield. AC test measurements for FLEX 10K devices are made under conditions equivalent to those shown in Figure 18. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 18. FLEX 10K AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 3.3-V devices or outputs. Numbers in brackets are for 2.5-V devices or outputs.



Operating Conditions

The following tables provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 5.0-V and 3.3-V FLEX 10K devices.

FLEX 10K 5.0-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		PQFP, TQFP, RQFP, and BGA packages, under bias		135	° C

FLEX 10K 5.0-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*Notes (3)*, *(4)*	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output buffers, 5.0-V operation	*Notes (3)*, *(4)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output buffers, 3.3-V operation	*Notes (3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
V_I	Input voltage		0	V_{CCINT}	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

FLEX 10K 5.0-V Device DC Operating Conditions *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CCINT} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 4.75 V, *Note (7)*	2.4			V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.00 V, *Note (7)*	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V, *Note (7)*	V_{CCIO} – 0.2			V
V_{OL}	5.0-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 4.75 V, *Note (8)*			0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V, *Note (8)*			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V, *Note (8)*			0.2	V
I_I	Input pin leakage current	V_I = V_{CC} or ground	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = V_{CC} or ground	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load		0.5	10	mA

5.0-V Device Capacitance of EPF10K10, EPF10K20 & EPF10K30 Devices *Note (9)*

Symbol	Parameter	Conditions	84-Pin PLCC EPF10K10		144-Pin TQFP EPF10K10 EPF10K20		208-Pin PQFP EPF10K10		208-Pin RQFP EPF10K20 EPF10K30		240-Pin RQFP EPF10K20 EPF10K30		356-Pin BGA EPF10K30		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8		8		8		8		8		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12		12		12		12		12		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8		8		8		8		8		8	pF

5.0-V Device Capacitance of EPF10K40, EPF10K50, EPF10K70 & EPF10K100 Devices *Note (9)*

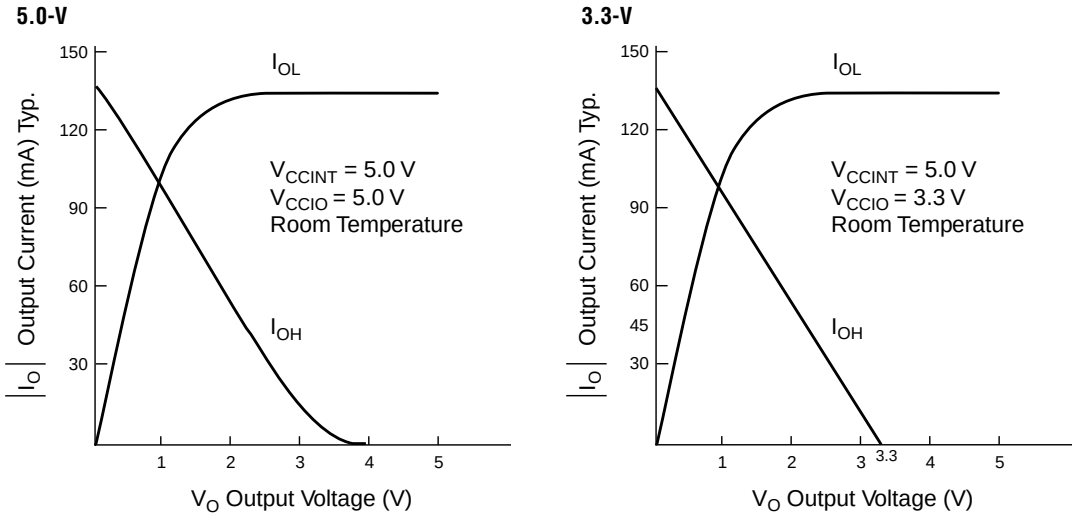
Symbol	Parameter	Conditions	208-Pin RQFP EPF10K40		240-Pin RQFP EPF10K40 EPF10K50 EPF10K70		356-Pin BGA EPF10K50		403-Pin PGA EPF10K50		503-Pin PGA EPF10K70 EPF10K100		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10		10		10		10		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		15		15		15		15		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10		10		10		10		10	pF

Notes to tables:

(1) See *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms. V_{CC} must rise monotonically.
(5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(6) These values are specified under "FLEX 10K 5.0-V Device Recommended Operating Conditions" on page 40.
(7) The I_{OH} parameter refers to high-level TTL or CMOS output current.
(8) The I_{OL} parameter refers to low-level TTL or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(9) Capacitance is sample-tested only.

Figure 19 shows the typical output drive characteristics of FLEX 10K devices with 5.0-V and 3.3-V V_{CCIO}. The output driver is compatible with the ***PCI Local Bus Specification, Revision 2.1*** (with 5.0-V V_{CCIO}.)

Figure 19. Output Drive Characteristics of FLEX 10K Devices



EPF10K50V & EPF10K130V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground	–0.5	4.6	V
V_I	DC input voltage	*Note (2)*	–2.0	5.7	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		RQFP and BGA packages, under bias		135	° C

EPF10K50V & EPF10K130V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*Notes (3), (4)*	3.00 (3.00)	3.60 (3.60)	V
V_{CCIO}	Supply voltage for output buffers	*Notes (3), (4)*	3.00 (3.00)	3.60 (3.60)	V
V_I	Input voltage	*Note (5)*	0	5.3	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

EPF10K50V & EPF10K130V Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		5.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, *Note (8)*	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, *Note (8)*	V_{CCIO}– 0.2			V
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 4 mA DC, *Note (9)*			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, *Note (9)*			0.2	V
I_I	Input pin leakage current	V_I = V_{CC} or ground	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = V_{CC} or ground	–10		10	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load		0.3		mA
		Note (10)		10		mA

EPF10K50V & EPF10K130V Device Capacitance *Note (11)*

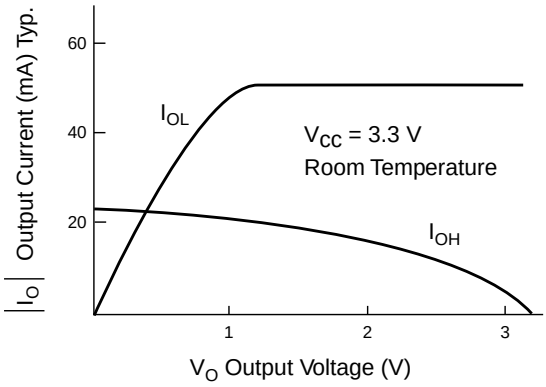
Symbol	Parameter	Conditions	240-Pin EPF10K50V		356-Pin BGA EPF10K50V		599-Pin PGA EPF10K130V		600-Pin PGA EPF10K130V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10		10		10		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		15		15		15		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10		10		10		10	pF

Notes to tables:

(1) See *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 5.7 V for periods shorter than 20 ns under no-load conditions.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms. V_{CC} must rise monotonically.
(5) Inputs of EPF10K50V and EPF10K130V devices may be driven before V_{CCINT} is powered.
(6) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.
(7) These values are specified under "FLEX 10K 3.3-V Device Recommended Operating Conditions" on page 45.
(8) The I_{OH} parameter refers to high-level TTL or CMOS output current.
(9) The I_{OL} parameter refers to low-level TTL or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(10) This parameter applies to -1 speed grade EPF10K50V devices.
(11) Capacitance is sample-tested only.

Figure 20 shows the typical output drive characteristics of EPF10K50V and EPF10K130V devices.

Figure 20. Output Drive Characteristics of EPF10K50V & EPF10K130V Devices



FLEX 10KA 3.3-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground, *Note (2)*	–0.5	4.6	V
V_I	DC input voltage		–2.0	5.7	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		PQFP, TQFP, RQFP, and BGA packages, under bias		135	° C

FLEX 10KA 3.3-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*Notes (3), (4)*	3.00 (3.00)	3.60 (3.60)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*Notes (3), (4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*Notes (3), (4)*	2.30 (2.30)	2.70 (2.70)	V
V_I	Input voltage	*Note (5)*	0	5.3	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

FLEX 10KA 3.3-V Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		1.7 or $0.5 \times V_{CCINT}$, whichever is lower		5.3	V
V_{IL}	Low-level input voltage		–0.5		$0.3 \times V_{CCINT}$	V
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.00 V, *Note (8)*	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V, *Note (8)*	V_{CCIO} – 0.2			V
	3.3-V high-level PCI output voltage	I_{OH} = –0.5 mA DC, V_{CCIO} = 3.00 to 3.60 V, *Note (8)*	$0.9 \times V_{CCIO}$			V
	2.5-V high-level output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 2.30 V, *Note (8)*	2.1			V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V, *Note (8)*	2.0			V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V, *Note (8)*	1.7			V
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 4 mA DC, V_{CCIO} = 3.00 V, *Note (9)*			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V, *Note (9)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V, *Note (9)*			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V, *Note (9)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V, *Note (9)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V, *Note (9)*			0.7	V
I_I	Input pin leakage current	$V_I = V_{CC}$ or ground	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CC}$ or ground	–10		10	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load		0.3		mA
		Note (10)		10		mA

3.3-V Device Capacitance of EPF10K10A & EPF10K30A Devices *Note (11), (12)*

Symbol	Parameter	Conditions	144-Pin TQFP EPF10K10A EPF10K30A		208-Pin RQFP EPF10K10A EPF10K30A		240-Pin RQFP EPF10K30A		356-Pin BGA EPF10K30A		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8		8		8		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12		12		12		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8		8		8		8	pF

3.3-V Device Capacitance of EPF10K100A Devices *Note (11), (12)*

Symbol	Parameter	Conditions	240-Pin RQFP EPF10K100A		356-Pin BGA EPF10K100A		Unit
			Min	Max	Min	Max	
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		15		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10		10	pF

3.3-V Device Capacitance of EPF10K250A Devices *Note (11), (12)*

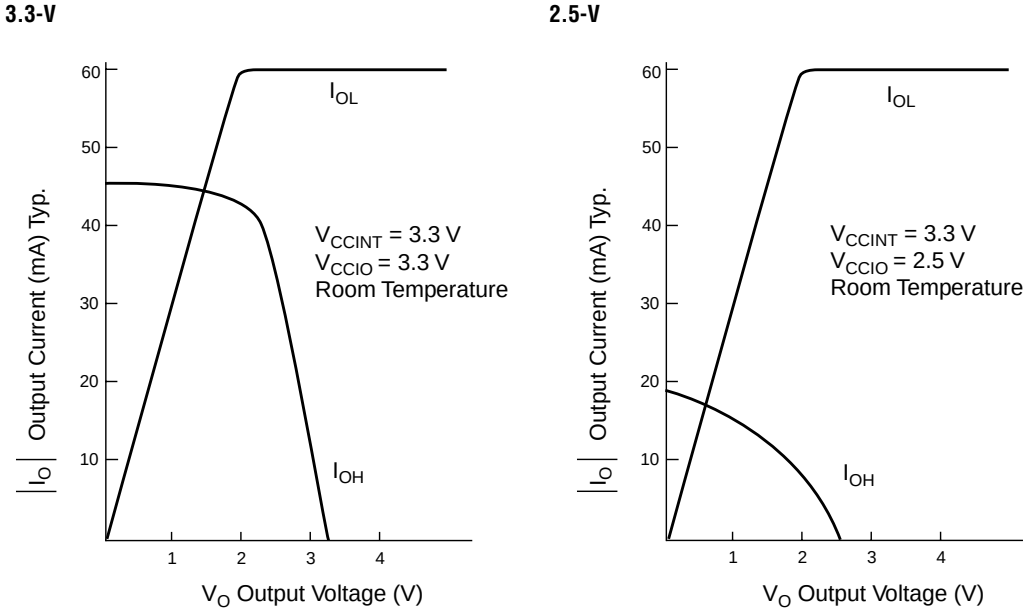
Symbol	Parameter	Conditions	599-Pin PGA EPF10K250A		600-Pin BGA EPF10K250A		Unit
			Min	Max	Min	Max	
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		15		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10		10	pF

Notes to tables:

(1) See *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.7 V for periods shorter than 20 ns under no-load conditions.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) Inputs of FLEX 10KA devices may be driven before V_{CCINT} and V_{CCIO} are powered.
(6) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.
(7) These values are specified under "FLEX 10K 3.3-V Device Recommended Operating Conditions" on page 45.
(8) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
(9) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(10) This parameter applies to EPF10K100A devices.
(11) Capacitance is sample-tested only.
(12) The information in this table is preliminary. For the most up-to-date information, contact Altera Applications.

Figure 21 shows the typical output drive characteristics of FLEX 10K devices with 3.3-V and 2.5-V V_{CCIO}. The output driver is compatible with the 3.3-V ***PCI Local Bus Specification, Revision 2.1*** (with 3.3-V V_{CCIO}.)

Figure 21. Output Drive Characteristics for FLEX 10KA Devices



Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Device performance can be estimated by following the signal path from a source, through the interconnect, to the destination. For example, the registered performance between two LEs on the same row can be calculated by adding the following parameters:

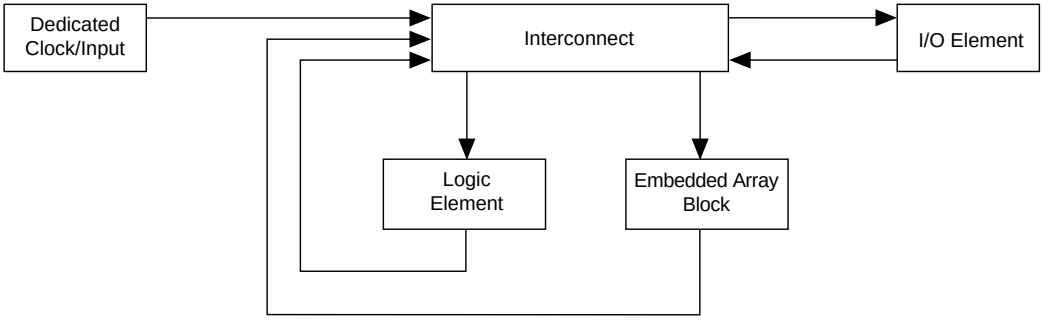
- LE register clock-to-output delay (t_{CO})
- Interconnect delay ($t_{SAMEROW}$)
- LE look-up table delay (t_{LUT})
- LE register setup time (t_{SU})

The routing delay depends on the placement of the source and destination LEs. A more complex registered path may involve multiple combinatorial LEs between the source and destination LEs.

Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 22 shows the overall timing model, which maps the possible paths to and from the various elements of the FLEX 10K device.

Figure 22. FLEX 10K Device Timing Model



Figures 23 through 25 show the delays that correspond to various paths and functions within the LE, IOE, and EAB timing models.

Figure 23. FLEX 10K Device LE Timing Model

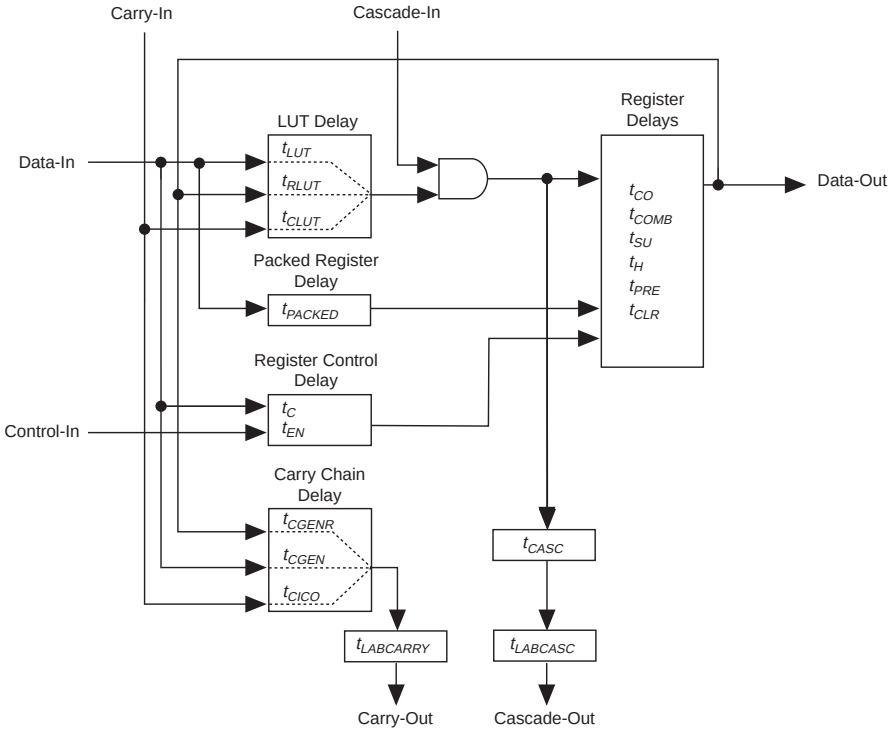


Figure 24. FLEX 10K Device IOE Timing Model

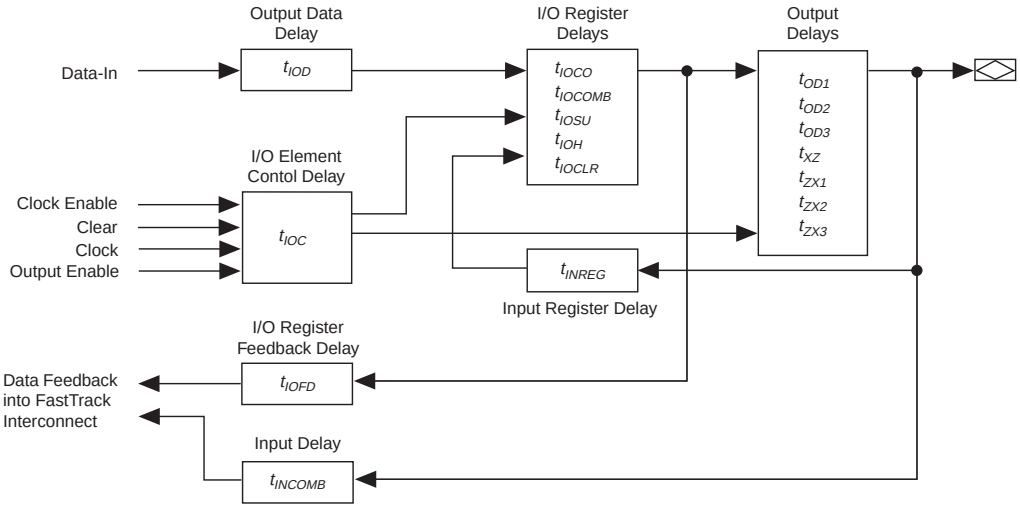
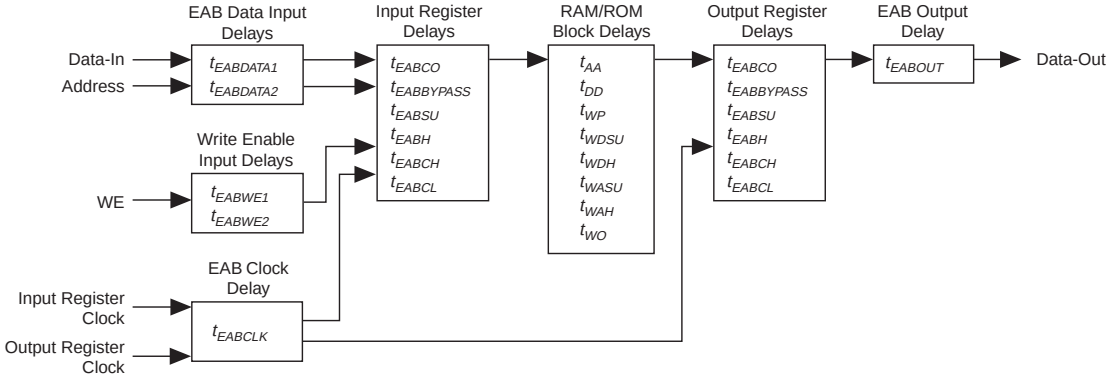


Figure 25. FLEX 10K Device EAB Timing Model



Tables 14 through 18 describe the FLEX 10K device internal timing parameters. These internal timing parameters are expressed as worst-case values. Using hand calculations, these parameters can be used to estimate design performance. However, before committing designs to silicon, actual worst-case performance should be modeled using timing simulation and analysis. Tables 19 and 20 describe FLEX 10K external timing parameters.

Table 14. LE Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
t_{LUT}	LUT delay for data-in	
t_{CLUT}	LUT delay for carry-in	
t_{RLUT}	LUT delay for LE register feedback	
t_{PACKED}	Data-in to packed register delay	
t_{EN}	LE register enable delay	
t_{CICO}	Carry-in to carry-out delay	
t_{CGEN}	Data-in to carry-out delay	
t_{CGENR}	LE register feedback to carry-out delay	
t_{CASC}	Cascade-in to cascade-out delay	
t_{C}	LE register control signal delay	
t_{CO}	LE register clock-to-output delay	
t_{COMB}	Combinatorial delay	
t_{SU}	LE register setup time before clock; LE register recovery time after asynchronous clear, preset, or load	
t_{H}	LE register hold time after clock	
t_{PRE}	LE register preset delay	
t_{CLR}	LE register clear delay	
t_{CH}	Minimum clock high time from clock pin	
t_{CL}	Minimum clock low time from clock pin	

Table 15. IOE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions
t_{IOD}	IOE data delay	
t_{IOC}	IOE register control signal delay	
t_{IOCO}	IOE register clock-to-output delay	
t_{IOCOMB}	IOE combinatorial delay	
t_{IOSU}	IOE register data setup time before clock; IOE register recovery time after asynchronous clear	
t_{IOH}	IOE register data hold time after clock	

Table 15. IOE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions
t_{IOCLR}	IOE register clear time	
t_{OD1}	Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$	C1 = 35 pF, *Note (2)*
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = low voltage	C1 = 35 pF, *Note (3)*
t_{OD3}	Output buffer and pad delay, slow slew rate = on	C1 = 35 pF, *Note (4)*
t_{XZ}	IOE output buffer disable delay	
t_{ZX1}	IOE output buffer enable delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$	C1 = 35 pF, *Note (2)*
t_{ZX2}	IOE output buffer enable delay, slow slew rate = off, V_{CCIO} = low voltage	C1 = 35 pF, *Note (3)*
t_{ZX3}	IOE output buffer enable delay, slow slew rate = on	C1 = 35 pF, *Note (4)*
t_{INREG}	IOE input pad and buffer to IOE register delay	
t_{IOFD}	IOE register feedback delay	
t_{INCOMB}	IOE input pad and buffer to FastTrack Interconnect delay	

Table 16. EAB Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions
$t_{EABDATA1}$	Data or address delay to EAB for combinatorial input	
$t_{EABDATA2}$	Data or address delay to EAB for registered input	
t_{EABWE1}	Write enable delay to EAB for combinatorial input	
t_{EABWE2}	Write enable delay to EAB for registered input	
t_{EABCLK}	EAB register clock delay	
t_{EABCO}	EAB register clock-to-output delay	
$t_{EABBYPASS}$	Bypass register delay	
t_{EABSU}	EAB register setup time before clock	
t_{EABH}	EAB register hold time after clock	
t_{EABCH}	Clock high time	
t_{EABCL}	Clock low time	
t_{AA}	Address access delay	
t_{WP}	Write pulse width	
t_{WDSU}	Data setup time before falling edge of write pulse	*Note (5)*
t_{WDH}	Data hold time after falling edge of write pulse	*Note (5)*
t_{WASU}	Address setup time before rising edge of write pulse	*Note (5)*

Table 16. EAB Timing Microparameters (Part 2 of 2) Note (1)		
Symbol	**Parameter**	**Conditions**
t_{WAH}	Address hold time after falling edge of write pulse	Note (5)
t_{WO}	Write enable to data output valid delay	
t_{DD}	Data-in to data-out valid delay	
t_{EABOUT}	Data-out delay	

Table 17. EAB Timing Macroparameters Notes (1), (6)		
Symbol	**Parameter**	**Conditions**
t_{EABAA}	EAB address access delay	
$t_{EABRCCOMB}$	EAB asynchronous read cycle time	
$t_{EABRCREG}$	EAB synchronous read cycle time	
t_{EABWP}	EAB write pulse width	
$t_{EABWCCOMB}$	EAB asynchronous write cycle time	
$t_{EABWCREG}$	EAB synchronous write cycle time	
t_{EABDD}	EAB data-in to data-out valid delay	
$t_{EABDATACO}$	EAB clock-to-output delay when using output registers	
$t_{EABDATASU}$	EAB data/address setup time before clock when using input register	
$t_{EABDATAH}$	EAB data/address hold time after clock when using input register	
$t_{EABWESU}$	EAB WE setup time before clock when using input register	
$t_{EABWESH}$	EAB WE hold time after clock when using input register	
$t_{EABWDSU}$	EAB data setup time before falling edge of write pulse when not using input registers	
t_{EABWDH}	EAB data hold time after falling edge of write pulse when not using input registers	
$t_{EABWASU}$	EAB address setup time before rising edge of write pulse when not using input registers	
t_{EABWAH}	EAB address hold time after falling edge of write pulse when not using input registers	
t_{EABWO}	EAB write enable to data output valid delay	

Table 18. Interconnect Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
$t_{SAMELAB}$	Routing delay for an LE driving another LE in the same LAB	
$t_{SAMEROW}$	Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row	*Note (7)*
$t_{SAMECOLUMN}$	Routing delay for an LE driving an IOE in the same column	*Note (7)*
$t_{DIFFROW}$	Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row	*Note (7)*
$t_{TWOROWS}$	Routing delay for a row IOE or EAB driving an LE or EAB in a different row	*Note (7)*
$t_{LEPERIPH}$	Routing delay for an LE driving a control signal of an IOE via the peripheral control bus	*Note (7)*
$t_{LABCARRY}$	Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	
$t_{DIN2IOE}$	Delay from dedicated input pin to IOE control input	*Note (7)*
t_{DIN2LE}	Delay from dedicated input pin to LE or EAB control input	*Note (7)*
$t_{DCLK2IOE}$	Delay from dedicated clock pin to IOE clock	*Note (7)*
$t_{DCLK2LE}$	Delay from dedicated clock pin to LE or EAB clock	*Note (7)*
$t_{DIN2DATA}$	Delay from dedicated input or clock to LE or EAB data	*Note (7)*

Table 19. External Reference Timing Parameters *Note (8)*

Symbol	Parameter	Conditions
t_{DRR}	Register-to-register delay via four LEs, three row interconnects, and four local interconnects	*Note (9)*

Table 20. External Timing Parameters *Note (10)*

Symbol	Parameter	Conditions
t_{INSU}	Setup time with global clock at IOE register	
t_{INH}	Hold time with global clock at IOE register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE register	
t_{ODH}	Output data hold time after clock	C1 = 35 pF, *Note (11)*

Notes to tables:

(1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.
(2) Operating conditions: V_{CCIO} = 5.0 V ± 5% for commercial use in FLEX 10K devices.
V_{CCIO} = 5.0 V ± 10% for industrial use in FLEX 10K devices.
V_{CCIO} = 3.3 V ± 10% for commercial or industrial use in FLEX 10KA devices.
(3) Operating conditions: V_{CCIO} = 3.3 V ± 10% for commercial or industrial use in FLEX 10K devices.
V_{CCIO} = 2.5 V ± 0.2 V for commercial or industrial use in FLEX 10KA devices.
(4) Operating conditions: V_{CCIO} = 2.5 V, 3.3 V, or 5.0 V.
(5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the WE signal is registered.
(6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.
(7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
(8) External reference timing parameters are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
(9) Contact Altera Applications for test circuit specifications and test conditions.
(10) These timing parameters are sample-tested only.
(11) This parameter is a guideline that is sample-tested only and based on extensive device characterization. This parameter applies for both global and non-global clocking and for LE, EAB, and IOE registers.

Figures 26 and 27 show the asynchronous and synchronous timing waveforms, respectively, for the EAB macroparameters in Table 16.

Figure 26. EAB Asynchronous Timing Waveforms

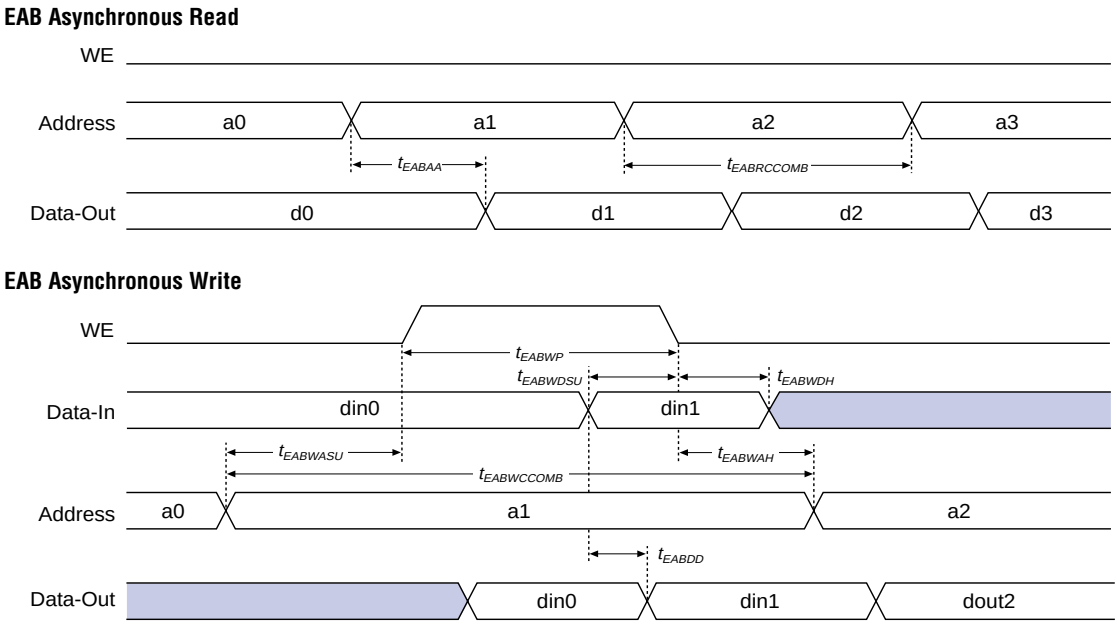
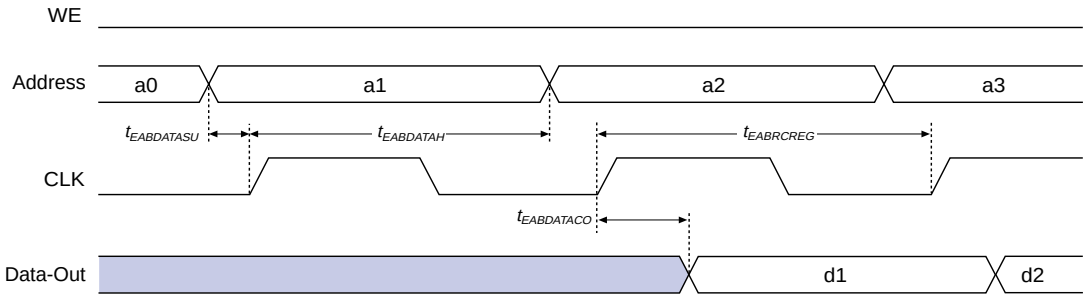
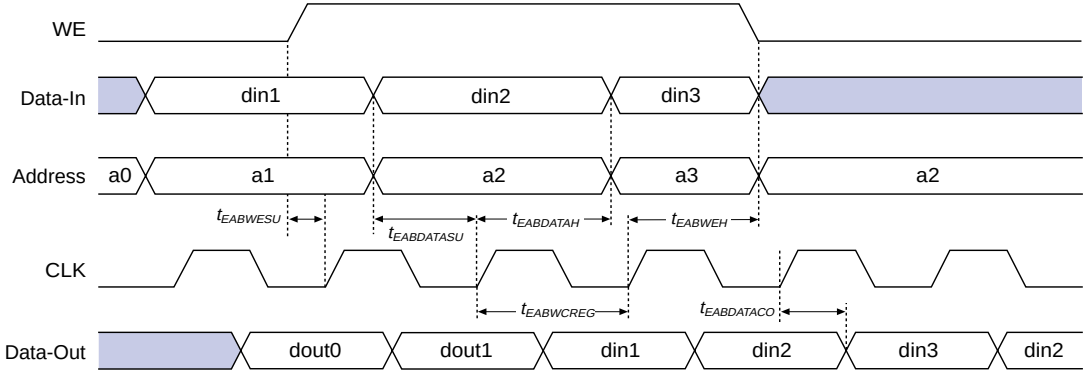


Figure 27. EAB Synchronous Timing Waveforms

EAB Synchronous Read



EAB Synchronous Write



EPF10K10 & EPF10K20 Device Internal & External Timing Parameters

EPF10K10 & EPF10K20 Device LE Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
t_{LUT}		1.4		1.7	ns
t_{CLUT}		0.6		0.7	ns
t_{RLUT}		1.5		1.9	ns
t_{PACKED}		0.6		0.9	ns
t_{EN}		1.0		1.2	ns
t_{CICO}		0.2		0.3	ns
t_{CGEN}		0.9		1.2	ns
t_{CGENR}		0.9		1.2	ns
t_{CASC}		0.8		0.9	ns
t_{C}		1.3		1.5	ns
t_{CO}		0.9		1.1	ns
t_{COMB}		0.5		0.6	ns
t_{SU}	1.3		2.5		ns
t_{H}	1.4		1.6		ns
t_{PRE}		1.0		1.2	ns
t_{CLR}		1.0		1.2	ns
t_{CH}	4.0		4.0		ns
t_{CL}	4.0		4.0		ns

Note:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.

EPF10K10 & EPF10K20 Device IOE Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
t_{IOD}		1.3		1.6	ns
t_{IOC}		0.5		0.7	ns
t_{IOCO}		0.2		0.2	ns
t_{IOCOMB}		0.0		0.0	ns
t_{IOSU}	2.8		3.2		ns
t_{IOH}	1.0		1.2		ns
t_{IOCLR}		1.0		1.2	ns
t_{OD1}		2.6		3.5	ns
t_{OD2}		4.9		6.4	ns
t_{OD3}		6.3		8.2	ns
t_{XZ}		4.5		5.4	ns
t_{ZX1}		4.5		5.4	ns
t_{ZX2}		6.8		8.3	ns
t_{ZX3}		8.2		10.1	ns
t_{INREG}		6.0		7.5	ns
t_{IOFD}		3.1		3.5	ns
t_{INCOMB}		3.1		3.5	ns

Note:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.

EPF10K10 & EPF10K20 Device EAB Internal Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{EABDATA1}$		1.5		1.9	ns
$t_{EABDATA2}$		4.8		6.0	ns
t_{EABWE1}		1.0		1.2	ns
t_{EABWE2}		5.0		6.2	ns
t_{EABCLK}		1.0		2.2	ns
t_{EABCO}		0.5		0.6	ns
$t_{EABBYPASS}$		1.5		1.9	ns
t_{EABSU}	1.5		1.8		ns
t_{EABH}	2.0		2.5		ns
t_{AA}		8.7		10.7	ns
t_{WP}	5.8		7.2		ns
t_{WDSU}	1.6		2.0		ns
t_{WDH}	0.3		0.4		ns
t_{WASU}	0.5		0.6		ns
t_{WAH}	1.0		1.2		ns
t_{WO}		5.0		6.2	ns
t_{DD}		5.0		6.2	ns
t_{EABOUT}		0.5		0.6	ns
t_{EABCH}	4.0		4.0		ns
t_{EABCL}	5.8		7.2		ns

Note:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.

EPF10K10 & EPF10K20 Device EAB Internal Timing Macroparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
t_{EABAA}		13.7		17.0	ns
$t_{EABRCCOMB}$	13.7		17.0		ns
$t_{EABRCREG}$	9.7		11.9		ns
t_{EABWP}	5.8		7.2		ns
$t_{EABWCCOMB}$	7.3		9.0		ns
$t_{EABWCREG}$	13.0		16.0		ns
t_{EABDD}		10.0		12.5	ns
$t_{EABDATACO}$		2.0		3.4	ns
$t_{EABDATASU}$	5.3		5.6		ns
$t_{EABDATAH}$	0.0		0.0		ns
$t_{EABWESU}$	5.5		5.8		ns
t_{EABWEH}	0.0		0.0		ns
$t_{EABWDSU}$	5.5		5.8		ns
t_{EABWDH}	0.0		0.0		ns
$t_{EABWASU}$	2.1		2.7		ns
t_{EABWAH}	0.0		0.0		ns
t_{EABWO}		9.5		11.8	ns

Note:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.

EPF10K10 Device Interconnect Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		4.8		6.2	ns
t_{DIN2LE}		2.6		3.8	ns
$t_{DIN2DATA}$		4.3		5.2	ns
$t_{DCLK2IOE}$		3.4		4.0	ns
$t_{DCLK2LE}$		2.6		3.8	ns
$t_{SAMELAB}$		0.6		0.6	ns
$t_{SAMEROW}$		3.6		3.8	ns
$t_{SAMECOLUMN}$		0.9		1.1	ns
$t_{DIFFROW}$		4.5		4.9	ns
$t_{TWOROWS}$		8.1		8.7	ns
$t_{LEPERIPH}$		3.3		3.9	ns
$t_{LABCARRY}$		0.5		0.8	ns
$t_{LABCASC}$		2.7		3.0	ns

EPF10K20 Device Interconnect Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		5.2		6.6	ns
t_{DIN2LE}		2.6		3.8	ns
$t_{DIN2DATA}$		4.3		5.2	ns
$t_{DCLK2IOE}$		4.3		4.0	ns
$t_{DCLK2LE}$		2.6		3.8	ns
$t_{SAMELAB}$		0.6		0.6	ns
$t_{SAMEROW}$		3.7		3.9	ns
$t_{SAMECOLUMN}$		1.4		1.6	ns
$t_{DIFFROW}$		5.1		5.5	ns
$t_{TWOROWS}$		8.8		9.4	ns
$t_{LEPERIPH}$		4.7		5.6	ns
$t_{LABCARRY}$		0.5		0.8	ns
$t_{LABCASC}$		2.7		3.0	ns

Note to tables:

(1) All timing parameters are described in Tables 14 through 20 in this data sheet.

EPF10K10 & EPF10K20 Device External Timing Parameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
t_{DRR}		16.1		20.0	ns
t_{INSU}, *Notes (2), (3)*	5.5		6.0		ns
t_{INH}, *Note (3)*	0.0		0.0		ns
t_{OUTCO}, *Note (3)*		6.7		8.4	ns
t_{ODH}, *Note (3)*	2.0		2.0		ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

EPF10K10A Device External Timing Parameters

EPF10K10 Device External Timing Parameters *(1), (2)*							
Symbol	-1 Speed Grade		-2 Speed Grade		-2 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{DRR}		9.0		10.4		12.2	ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These timing parameters are preliminary. For the most up-to-date information, contact Altera Applications at (800) 800-EPLD.

EPF10K30, EPF10K40 & EPF10K50 Device Internal & External Timing Parameters

EPF10K30, EPF10K40 & EPF10K50 Device LE Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
t_{LUT}		1.3		1.8	ns
t_{CLUT}		0.6		0.6	ns
t_{RLUT}		1.5		2.0	ns
t_{PACKED}		0.5		0.8	ns
t_{EN}		0.9		1.5	ns
t_{CICO}		0.2		0.4	ns
t_{CGEN}		0.9		1.4	ns
t_{CGENR}		0.9		1.4	ns
t_{CASC}		1.0		1.2	ns
t_{C}		1.3		1.6	ns
t_{CO}		0.9		1.2	ns
t_{COMB}		0.6		0.6	ns
t_{SU}	1.4		1.4		ns
t_{H}	0.9		1.3		ns
t_{PRE}		0.9		1.2	ns
t_{CLR}		0.9		1.2	ns
t_{CH}	4.0		4.0		ns
t_{CL}	4.0		4.0		ns

Note:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.

EPF10K30, EPF10K40 & EPF10K50 Device IOE Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
t_{IOD}		0.4		0.6	ns
t_{IOC}		0.5		0.9	ns
t_{IOCO}		0.4		0.5	ns
t_{IOCOMB}		0.0		0.0	ns
t_{IOSU}	3.1		3.5		ns
t_{IOH}	1.0		1.9		ns
t_{IOCLR}		1.0		1.2	ns
t_{OD1}		3.3		3.6	ns
t_{OD2}		5.6		6.5	ns
t_{OD3}		7.0		8.3	ns
t_{XZ}		5.2		5.5	ns
t_{ZX1}		5.2		5.5	ns
t_{ZX2}		7.5		8.4	ns
t_{ZX3}		8.9		10.2	ns
t_{INREG}		7.7		10.0	ns
t_{IOFD}		3.3		4.0	ns
t_{INCOMB}		3.3		4.0	ns

Note:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.

EPF10K30, EPF10K40 & EPF10K50 Device EAB Internal Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{EABDATA1}$		1.5		1.9	ns
$t_{EABDATA2}$		4.8		6.0	ns
t_{EABWE1}		1.0		1.2	ns
t_{EABWE2}		5.0		6.2	ns
t_{EABCLK}		1.0		2.2	ns
t_{EABCO}		0.5		0.6	ns
$t_{EABBYPASS}$		1.5		1.9	ns
t_{EABSU}	1.5		1.8		ns
t_{EABH}	2.0		2.5		ns
t_{AA}		8.7		10.7	ns
t_{WP}	5.8		7.2		ns
t_{WDSU}	1.6		2.0		ns
t_{WDH}	0.3		0.4		ns
t_{WASU}	0.5		0.6		ns
t_{WAH}	1.0		1.2		ns
t_{WO}		5.0		6.2	ns
t_{DD}		5.0		6.2	ns
t_{EABOUT}		0.5		0.6	ns
t_{EABCH}	4.0		4.0		ns
t_{EABCL}	5.8		7.2		ns

Note:

(1) All timing parameters are described in Tables 14 through 20 in this data sheet.

EPF10K30, EPF10K40 & EPF10K50 Device EAB Internal Timing Macroparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
t_{EABAA}		13.7		17.0	ns
$t_{EABRCCOMB}$	13.7		17.0		ns
$t_{EABRCREG}$	9.7		11.9		ns
t_{EABWP}	5.8		7.2		ns
$t_{EABWCCOMB}$	7.3		9.0		ns
$t_{EABWCREG}$	13.0		16.0		ns
t_{EABDD}		10.0		12.5	ns
$t_{EABDATACO}$		2.0		3.4	ns
$t_{EABDATASU}$	5.3		5.6		ns
$t_{EABDATAH}$	0.0		0.0		ns
$t_{EABWESU}$	5.5		5.8		ns
t_{EABWEH}	0.0		0.0		ns
$t_{EABWDSU}$	5.5		5.8		ns
t_{EABWDH}	0.0		0.0		ns
$t_{EABWASU}$	2.1		2.7		ns
t_{EABWAH}	0.0		0.0		ns
t_{EABWO}		9.5		11.8	ns

Note:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.

EPF10K30 Device Interconnect Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		6.9		8.7	ns
t_{DIN2LE}		3.6		4.8	ns
$t_{DIN2DATA}$		5.5		7.2	ns
$t_{DCLK2IOE}$		4.6		6.2	ns
$t_{DCLK2LE}$		3.6		4.8	ns
$t_{SAMELAB}$		0.3		0.3	ns
$t_{SAMEROW}$		3.3		3.7	ns
$t_{SAMECOLUMN}$		2.5		2.7	ns
$t_{DIFFROW}$		5.8		6.4	ns
$t_{TWOROWS}$		9.1		10.1	ns
$t_{LEPERIPH}$		6.2		7.1	ns
$t_{LABCARRY}$		0.4		0.6	ns
$t_{LABCASC}$		2.4		3.0	ns

EPF10K40 Device Interconnect Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		7.6		9.4	ns
t_{DIN2LE}		3.6		4.8	ns
$t_{DIN2DATA}$		5.5		7.2	ns
$t_{DCLK2IOE}$		4.6		6.2	ns
$t_{DCLK2LE}$		3.6		4.8	ns
$t_{SAMELAB}$		0.3		0.3	ns
$t_{SAMEROW}$		3.3		3.7	ns
$t_{SAMECOLUMN}$		3.1		3.2	ns
$t_{DIFFROW}$		6.4		6.4	ns
$t_{TWOROWS}$		9.7		10.6	ns
$t_{LEPERIPH}$		6.4		7.1	ns
$t_{LABCARRY}$		0.4		0.6	ns
$t_{LABCASC}$		2.4		3.0	ns

Note to tables:

(1) All timing parameters are described in Tables 14 through 20 in this data sheet.

EPF10K50 Device Interconnect Timing Microparameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		8.4		10.2	ns
t_{DIN2LE}		3.6		4.8	ns
$t_{DIN2DATA}$		5.5		7.2	ns
$t_{DCLK2IOE}$		4.6		6.2	ns
$t_{DCLK2LE}$		3.6		4.8	ns
$t_{SAMELAB}$		0.3		0.3	ns
$t_{SAMEROW}$		3.3		3.7	ns
$t_{SAMECOLUMN}$		3.9		4.1	ns
$t_{DIFFROW}$		7.2		7.8	ns
$t_{TWOROWS}$		10.5		11.5	ns
$t_{LEPERIPH}$		7.5		8.2	ns
$t_{LABCARRY}$		0.4		0.6	ns
$t_{LABCASC}$		2.4		3.0	ns

EPF10K30, EPF10K40 & EPF10K50 Device External Timing Parameters *Note (1)*					
Symbol	-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	
t_{DRR}		17.2		21.1	ns
t_{INSU}, *Notes (2), (3)*	5.7		6.4		ns
t_{INH}, *Note (3)*	0.0		0.0		ns
t_{OUTCO}, *Note (3)*		8.8		11.2	ns
t_{ODH}, *Note (3)*	2.0		2.0		ns

Notes to tables:

(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

EPF10K70 Device Internal & External Timing Parameters

EPF10K70 Device LE Timing Microparameters *Note (1)*							
Symbol	-2 Speed Grade, *Note (2)*		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{LUT}		1.3		1.5		2.0	ns
t_{CLUT}		0.4		0.4		0.5	ns
t_{RLUT}		1.5		1.6		2.0	ns
t_{PACKED}		0.8		0.9		1.3	ns
t_{EN}		0.8		0.9		1.2	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		1.0		1.1		1.4	ns
t_{CGENR}		1.1		1.2		1.5	ns
t_{CASC}		1.0		1.1		1.3	ns
t_{C}		0.7		0.8		1.0	ns
t_{CO}		0.9		1.0		1.4	ns
t_{COMB}		0.4		0.5		0.7	ns
t_{SU}	1.9		2.1		2.6		ns
t_{H}	2.1		2.3		3.1		ns
t_{PRE}		0.9		1.0		1.4	ns
t_{CLR}		0.9		1.0		1.4	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.

EPF10K70 Device IOE Timing Microparameters *Note (1)*							
Symbol	-2 Speed Grade, *Note (2)*		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		0.0		0.0		0.0	ns
t_{IOC}		0.4		0.5		0.7	ns
t_{IOCO}		0.4		0.4		0.9	ns
t_{IOCOMB}		0.0		0.0		0.0	ns
t_{IOSU}	4.5		5.0		6.2		ns
t_{IOH}	0.4		0.5		0.7		ns
t_{IOCLR}		0.6		0.7		1.6	ns
t_{OD1}		3.6		4.0		5.0	ns
t_{OD2}		5.6		6.3		7.3	ns
t_{OD3}		6.9		7.7		8.7	ns
t_{XZ}		5.5		6.2		6.8	ns
t_{ZX1}		5.5		6.2		6.8	ns
t_{ZX2}		7.5		8.5		9.1	ns
t_{ZX3}		8.8		9.9		10.5	ns
t_{INREG}		8.0		9.0		10.2	ns
t_{IOFD}		7.2		8.1		10.3	ns
t_{INCOMB}		7.2		8.1		10.3	ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.

EPF10K70 Device EAB Internal Microparameters *Note (1)*							
Symbol	-2 Speed Grade, *Note (2)*		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{EABDATA1}$		1.3		1.5		1.9	ns
$t_{EABDATA2}$		4.3		4.8		6.0	ns
t_{EABWE1}		0.9		1.0		1.2	ns
t_{EABWE2}		4.5		5.0		6.2	ns
t_{EABCLK}		0.9		1.0		2.2	ns
t_{EABCO}		0.4		0.5		0.6	ns
$t_{EABBYPASS}$		1.3		1.5		1.9	ns
t_{EABSU}	1.3		1.5		1.8		ns
t_{EABH}	1.8		2.0		2.5		ns
t_{AA}		7.8		8.7		10.7	ns
t_{WP}	5.2		5.8		7.2		ns
t_{WDSU}	1.4		1.6		2.0		ns
t_{WDH}	0.3		0.3		0.4		ns
t_{WASU}	0.4		0.5		0.6		ns
t_{WAH}	0.9		1.0		1.2		ns
t_{WO}		4.5		5.0		6.2	ns
t_{DD}		4.5		5.0		6.2	ns
t_{EABOUT}		0.4		0.5		0.6	ns
t_{EABCH}	4.0		4.0		4.0		ns
t_{EABCL}	4.0		4.0		4.0		ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.

EPF10K70 Device EAB Internal Timing Macroparameters *Note (1)*							
Symbol	-2 Speed Grade, *Note (2)*		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		12.1		13.7		17.0	ns
$t_{EABRCCOMB}$	12.1		13.7		17.0		ns
$t_{EABRCREG}$	8.6		9.7		11.9		ns
t_{EABWP}	5.2		5.8		7.2		ns
$t_{EABWCCOMB}$	6.5		7.3		9.0		ns
$t_{EABWCREG}$	11.6		13.0		16.0		ns
t_{EABDD}		8.8		10.0		12.5	ns
$t_{EABDATACO}$		1.7		2.0		3.4	ns
$t_{EABDATASU}$	4.7		5.3		5.6		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	4.9		5.5		5.8		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.8		2.1		2.7		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	4.1		4.7		5.8		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		8.4		9.5		11.8	ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.

EPF10K70 Device Interconnect Timing Microparameters *Note (1)*							
Symbol	-2 Speed Grade, *Note (2)*		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		6.6		7.3		8.8	ns
t_{DIN2LE}		4.2		4.8		6.0	ns
$t_{DIN2DATA}$		6.5		7.1		10.8	ns
$t_{DCLK2IOE}$		5.5		6.2		7.7	ns
$t_{DCLK2LE}$		4.2		4.8		6.0	ns
$t_{SAMELAB}$		0.4		0.4		0.5	ns
$t_{SAMEROW}$		4.8		4.9		5.5	ns
$t_{SAMECOLUMN}$		3.3		3.4		3.7	ns
$t_{DIFFROW}$		8.1		8.3		9.2	ns
$t_{TWOROWS}$		12.9		13.2		14.7	ns
$t_{LEPERIPH}$		5.5		5.7		6.5	ns
$t_{LABCARRY}$		0.8		0.9		1.1	ns
$t_{LABCASC}$		2.7		3.0		3.2	ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.

EPF10K70 Device External Timing Parameters *Note (1)*							
Symbol	-2 Speed Grade, *Note (2)*		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{DRR}		17.2		19.1		24.2	ns
t_{INSU}, *Notes (3)*, *(4)*	6.6		7.3		8.0		ns
t_{INH}, *Note (4)*	0.0		0.0		0.0		ns
t_{OUTCO}, *Note (4)*		9.9		11.1		14.3	ns
t_{ODH}, *Note (4)*	2.0		2.0		2.0		ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.
(3) Using an LE to register the signal may provide a lower setup time.
(4) This parameter is specified by characterization.

EPF10K100 Device Internal & External Timing Parameters

EPF10K100 Device LE Timing Microparameters *Note (1)*							
Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{LUT}		1.5		1.5		2.0	ns
t_{CLUT}		0.4		0.4		0.5	ns
t_{RLUT}		1.6		1.6		2.0	ns
t_{PACKED}		0.9		0.9		1.3	ns
t_{EN}		0.9		0.9		1.2	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		1.1		1.1		1.4	ns
t_{CGENR}		1.2		1.2		1.5	ns
t_{CASC}		1.1		1.1		1.3	ns
t_{C}		0.8		0.8		1.0	ns
t_{CO}		1.0		1.0		1.4	ns
t_{COMB}		0.5		0.5		0.7	ns
t_{SU}	2.1		2.1		2.6		ns
t_{H}	2.3		2.3		3.1		ns
t_{PRE}		1.0		1.0		1.4	ns
t_{CLR}		1.0		1.0		1.4	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns

Note:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.

EPF10K100 Device IOE Timing Microparameters *Note (1)*							
Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		0.0		0.0		0.0	ns
t_{IOC}		0.5		0.5		0.7	ns
t_{IOCO}		0.4		0.4		0.9	ns
t_{IOCOMB}		0.0		0.0		0.0	ns
t_{IOSU}	5.5		5.5		6.7		ns
t_{IOH}	0.5		0.5		0.7		ns
t_{IOCLR}		0.7		0.7		1.6	ns
t_{OD1}		4.0		4.0		5.0	ns
t_{OD2}		6.3		6.3		7.3	ns
t_{OD3}		7.7		7.7		8.7	ns
t_{XZ}		6.2		6.2		6.8	ns
t_{ZX1}		6.2		6.2		6.8	ns
t_{ZX2}		8.5		8.5		9.1	ns
t_{ZX3}		9.9		9.9		10.5	ns
t_{INREG} without ClockLock or ClockBoost circuitry		9.0		9.0		10.5	ns
t_{INREG} with ClockLock or ClockBoost circuitry		3.0		–		–	ns
t_{IOFD}		8.1		8.1		10.3	ns
t_{INCOMB}		8.1		8.1		10.3	ns

Note:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.

EPF10K100 Device EAB Internal Microparameters *Note (1)*							
Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{EABDATA1}$		1.5		1.5		1.9	ns
$t_{EABDATA2}$		4.8		4.8		6.0	ns
t_{EABWE1}		1.0		1.0		1.2	ns
t_{EABWE2}		5.0		5.0		6.2	ns
t_{EABCLK}		1.0		1.0		2.2	ns
t_{EABCO}		0.5		0.5		0.6	ns
$t_{EABBYPASS}$		1.5		1.5		1.9	ns
t_{EABSU}	1.5		1.5		1.8		ns
t_{EABH}	2.0		2.0		2.5		ns
t_{AA}		8.7		8.7		10.7	ns
t_{WP}	5.8		5.8		7.2		ns
t_{WDSU}	1.6		1.6		2.0		ns
t_{WDH}	0.3		0.3		0.4		ns
t_{WASU}	0.5		0.5		0.6		ns
t_{WAH}	1.0		1.0		1.2		ns
t_{WO}		5.0		5.0		6.2	ns
t_{DD}		5.0		5.0		6.2	ns
t_{EABOUT}		0.5		0.5		0.6	ns
t_{EABCH}	4.0		4.0		4.0		ns
t_{EABCL}	5.8		5.8		7.2		ns

Note:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.

EPF10K100 Device EAB Internal Timing Macroparameters *Note (1)*							
Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		13.7		13.7		17.0	ns
$t_{EABRCCOMB}$	13.7		13.7		17.0		ns
$t_{EABRCREG}$	9.7		9.7		11.9		ns
t_{EABWP}	5.8		5.8		7.2		ns
$t_{EABWCCOMB}$	7.3		7.3		9.0		ns
$t_{EABWCREG}$	13.0		13.0		16.0		ns
t_{EABDD}		10.0		10.0		12.5	ns
$t_{EABDATACO}$		2.0		2.0		3.4	ns
$t_{EABDATASU}$	5.3		5.3		5.6		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	5.5		5.5		5.8		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	5.5		5.5		5.8		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	2.1		2.1		2.7		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		9.5		9.5		11.8	ns

Note:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.

EPF10K100 Device Interconnect Timing Microparameters *Note (1)*							
Symbol	-3 Speed Grade		-4 Speed Grade		-3 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		10.3		10.3		12.2	ns
t_{DIN2LE}		4.8		4.8		6.0	ns
$t_{DIN2DATA}$		7.3		7.3		11.0	ns
$t_{DCLK2IOE}$ without ClockLock or ClockBoost circuitry		6.2		6.2		7.7	ns
$t_{DCLK2IOE}$ with ClockLock or ClockBoost circuitry		2.3		–		–	ns
$t_{DCLK2LE}$ without ClockLock or ClockBoost circuitry		4.8		4.8		6.0	ns
$t_{DCLK2LE}$ with ClockLock or ClockBoost circuitry		2.3		–		–	ns
$t_{SAMELAB}$		0.4		0.4		0.5	ns
$t_{SAMEROW}$		4.9		4.9		5.5	ns
$t_{SAMECOLUMN}$		5.1		5.1		5.4	ns
$t_{DIFFROW}$		10.0		10.0		10.9	ns
$t_{TWOROWS}$		14.9		14.9		16.4	ns
$t_{LEPERIPH}$		6.9		6.9		8.1	ns
$t_{LABCARRY}$		0.9		0.9		1.1	ns
$t_{LABCASC}$		3.0		3.0		3.2	ns

Note:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.

EPF10K100 Device External Timing Parameters *Note (1)*							
Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{DRR}		19.1		19.1		24.2	ns
t_{INSU}, without ClockLock or ClockBoost circuitry *Notes (2)*, *(3)*	7.8		7.8		8.5		ns
t_{INSU}, with ClockLock or ClockBoost circuitry *Notes (2)*, *(3)*	6.2						ns
t_{INH}, *Note (3)*	0.0		0.0		0.0		ns
t_{OUTCO}, without ClockLock or ClockBoost circuitry *Notes (3)*		11.1		11.1		14.3	ns
t_{OUTCO}, with ClockLock or ClockBoost circuitry *Note (3)*		6.7					ns
t_{ODH}, *Note (3)*	2.0		2.0		2.0		ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

EPF10K50V Device Internal & External Timing Parameters

EPF10K50V Device LE Timing Microparameters *Note (1)*							
Symbol	-2 Speed Grade, *Note (2)*		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{LUT}		1.0		1.3		1.6	ns
t_{CLUT}		0.5		0.6		0.6	ns
t_{RLUT}		0.8		0.9		1.0	ns
t_{PACKED}		0.4		0.5		0.7	ns
t_{EN}		0.9		1.1		1.4	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		0.7		0.8		1.2	ns
t_{CGENR}		0.3		0.3		0.4	ns
t_{CASC}		0.7		0.8		0.9	ns
t_{C}		1.0		1.3		1.5	ns
t_{CO}		0.7		0.9		1.0	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	1.6		2.2		2.5		ns
t_{H}	0.8		1.0		1.4		ns
t_{PRE}		0.4		0.5		0.5	ns
t_{CLR}		0.4		0.5		0.5	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.

EPF10K50V Device IOE Timing Microparameters *Note (1)*							
Symbol	-2 Speed Grade, *Note (2)*		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		1.6		1.9		2.1	ns
t_{IOC}		0.4		0.5		0.5	ns
t_{IOCO}		0.3		0.4		0.4	ns
t_{IOCOMB}		0.0		0.0		0.0	ns
t_{IOSU}	2.8		3.4		3.9		ns
t_{IOH}	0.8		1.0		1.4		ns
t_{IOCLR}		0.6		0.7		0.7	ns
t_{OD1}		3.2		3.9		4.7	ns
t_{OD2}		–		–		–	ns
t_{OD3}		6.9		7.6		8.4	ns
t_{XZ}		3.1		3.8		4.6	ns
t_{ZX1}		3.1		3.8		4.6	ns
t_{ZX2}		–		–		–	ns
t_{ZX3}		6.8		7.5		8.3	ns
t_{INREG}		5.7		7.0		9.0	ns
t_{IOFD}		1.9		2.3		2.7	ns
t_{INCOMB}		1.9		2.3		2.7	ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.

EPF10K50V Device EAB Internal Microparameters *Note (1)*							
Symbol	-2 Speed Grade, *Note (2)*		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{EABDATA1}$		2.8		3.4		4.6	ns
$t_{EABDATA2}$		3.9		4.8		5.9	ns
t_{EABWE1}		2.5		3.0		3.7	ns
t_{EABWE2}		4.1		5.0		6.2	ns
t_{EABCLK}		0.8		1.0		1.2	ns
t_{EABCO}		0.2		0.3		0.4	ns
$t_{EABBYPASS}$		1.1		1.3		1.6	ns
t_{EABSU}	1.5		1.8		2.2		ns
t_{EABH}	1.6		2.0		2.5		ns
t_{AA}		8.2		10.0		12.4	ns
t_{WP}	4.9		6.0		7.4		ns
t_{WDSU}	0.8		1.0		1.2		ns
t_{WDH}	0.2		0.3		0.4		ns
t_{WASU}	0.4		0.5		0.6		ns
t_{WAH}	0.8		1.0		1.2		ns
t_{WO}		4.3		5.3		6.5	ns
t_{DD}		4.3		5.3		6.5	ns
t_{EABOUT}		0.4		0.5		0.6	ns
t_{EABCH}	4.0		4.0		4.0		ns
t_{EABCL}	4.0		4.0		4.0		ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.

EPF10K50V Device EAB Internal Timing Macroparameters *Note (1)*							
Symbol	-2 Speed Grade, *Note (2)*		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		13.6		16.5		20.8	ns
$t_{EABRCCOMB}$	13.6		16.5		20.8		ns
$t_{EABRCREG}$	8.8		10.8		13.4		ns
t_{EABWP}	4.9		6.0		7.4		ns
$t_{EABWCCOMB}$	6.1		7.5		9.2		ns
$t_{EABWCREG}$	11.6		14.2		17.4		ns
t_{EABDD}		9.7		11.8		14.9	ns
$t_{EABDATACO}$		1.4		1.8		2.2	ns
$t_{EABDATASU}$	4.6		5.6		6.9		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	4.8		5.8		7.2		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.1		1.4		2.1		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	4.6		5.6		7.4		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		9.4		11.4		14.0	ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.

EPF10K50V Device Interconnect Timing Microparameters *Note (1)*							
Symbol	-2 Speed Grade, *Note (2)*		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		6.0		7.2		8.2	ns
t_{DIN2LE}		2.6		3.1		3.9	ns
$t_{DIN2DATA}$		5.7		6.6		7.5	ns
$t_{DCLK2IOE}$		3.9		4.8		5.5	ns
$t_{DCLK2LE}$		2.6		3.1		3.9	ns
$t_{SAMELAB}$		0.2		0.3		0.3	ns
$t_{SAMEROW}$		2.9		4.3		3.9	ns
$t_{SAMECOLUMN}$		3.6		3.4		2.7	ns
$t_{DIFFROW}$		6.5		7.7		6.6	ns
$t_{TWOROWS}$		9.4		12.0		10.5	ns
$t_{LEPERIPH}$		5.0		5.7		6.5	ns
$t_{LABCARRY}$		0.4		0.5		0.7	ns
$t_{LABCASC}$		1.3		1.6		2.0	ns

EPF10K50V Device External Timing Parameters *Note (1)*									
Symbol	-1 Speed Grade, *Note (2)*		-2 Speed Grade, *Note (3)*		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{DRR}		11.2		14.0		17.2		21.1	ns
t_{INSU}, *Notes (3), (4)*			4.2		5.2		6.9		ns
t_{INH}, *Note (4)*			0.0		0.0		0.0		ns
t_{OUTCO}, *Note (4)*				7.8		9.5		11.1	ns
t_{ODH}, *Note (4)*			2.0		2.0		2.0		ns

Notes:

(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) The -1 speed grade is under development. Contact your local Altera sales representative for availability.
(3) These parameters are preliminary. For the most up-to-date information, contact Altera Applications at (800) 800-EPLD.
(4) This parameter is specified by characterization.

EPF10K130V Device Internal & External Timing Parameters

EPF10K130V Device LE Timing Microparameters *Notes (1), (2)*							
Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{LUT}		1.3		1.8		2.3	ns
t_{CLUT}		0.5		0.7		0.9	ns
t_{RLUT}		1.2		1.7		2.2	ns
t_{PACKED}		0.5		0.6		0.7	ns
t_{EN}		0.6		0.8		1.0	ns
t_{CICO}		0.2		0.3		0.4	ns
t_{CGEN}		0.3		0.4		0.5	ns
t_{CGENR}		0.7		1.0		1.3	ns
t_{CASC}		0.9		1.2		1.5	ns
t_{C}		1.9		2.4		3.0	ns
t_{CO}		0.6		0.9		1.1	ns
t_{COMB}		0.5		0.7		0.9	ns
t_{SU}	0.2		0.2		0.3		ns
t_{H}	0.0		0.0		0.0		ns
t_{PRE}		2.4		3.1		3.9	ns
t_{CLR}		2.4		3.1		3.9	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.

EPF10K130V Device IOE Timing Microparameters *Notes (1), (2)*							
Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		1.3		1.6		2.0	ns
t_{IOC}		0.4		0.5		0.7	ns
t_{IOCO}		0.3		0.4		0.5	ns
t_{IOCOMB}		0.0		0.0		0.0	ns
t_{IOSU}	2.6		3.3		3.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.7		2.2		2.7	ns
t_{OD1}		3.5		4.4		5.0	ns
t_{OD2}		–		–		–	ns
t_{OD3}		8.2		8.1		9.7	ns
t_{XZ}		4.9		6.3		7.4	ns
t_{ZX1}		4.9		6.3		7.4	ns
t_{ZX2}		–		–		–	ns
t_{ZX3}		9.6		10.0		12.1	ns
t_{INREG}		7.9		10.0		12.6	ns
t_{IOFD}		6.2		7.9		9.9	ns
t_{INCOMB}		6.2		7.9		9.9	ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.

EPF10K130V Device EAB Internal Microparameters *Note (1), (2)*							
Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{EABDATA1}$		1.9		2.4		2.4	ns
$t_{EABDATA2}$		3.7		4.7		4.7	ns
t_{EABWE1}		1.9		2.4		2.4	ns
t_{EABWE2}		3.7		4.7		4.7	ns
t_{EABCLK}		0.7		0.9		0.9	ns
t_{EABCO}		0.5		0.6		0.6	ns
$t_{EABBYPASS}$		0.6		0.8		0.8	ns
t_{EABSU}	1.4		1.8		1.8		ns
t_{EABH}	0.0		0.0		0.0		ns
t_{AA}		5.6		7.1		7.1	ns
t_{WP}	3.7		4.7		4.7		ns
t_{WDSU}	4.6		5.9		5.9		ns
t_{WDH}	0.0		0.0		0.0		ns
t_{WASU}	3.9		5.0		5.0		ns
t_{WAH}	0.0		0.0		0.0		ns
t_{WO}		5.6		7.1		7.1	ns
t_{DD}		5.6		7.1		7.1	ns
t_{EABOUT}		2.4		3.1		3.1	ns
t_{EABCH}	4.0		4.0		4.0		ns
t_{EABCL}	4.0		4.7		4.7		ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.

EPF10K130V Device EAB Internal Timing Macroparameters *Notes (1), (2)*							
Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		11.2		14.2		14.2	ns
$t_{EABRCCOMB}$	11.1		14.2		14.2		ns
$t_{EABRCREG}$	8.5		10.8		10.8		ns
t_{EABWP}	3.7		4.7		4.7		ns
$t_{EABWCCOMB}$	7.6		9.7		9.7		ns
$t_{EABWCREG}$	14.0		17.8		17.8		ns
t_{EABDD}		11.1		14.2		14.2	ns
$t_{EABDATACO}$		3.6		4.6		4.6	ns
$t_{EABDATASU}$	4.4		5.6		5.6		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	4.4		5.6		5.6		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	4.6		5.9		5.9		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.9		5.0		5.0		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		11.1		14.2		14.2	ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.

EPF10K130V Device Interconnect Timing Microparameters *Notes (1), (2)*							
Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		8.0		9.0		9.5	ns
t_{DIN2LE}		2.4		3.0		3.1	ns
$t_{DIN2DATA}$		5.0		6.3		7.4	ns
$t_{DCLK2IOE}$		3.6		4.6		5.1	ns
$t_{DCLK2LE}$		2.4		3.0		3.1	ns
$t_{SAMELAB}$		0.4		0.6		0.8	ns
$t_{SAMEROW}$		4.5		5.3		6.5	ns
$t_{SAMECOLUMN}$		9.0		9.5		9.7	ns
$t_{DIFFROW}$		13.5		14.8		16.2	ns
$t_{TWOROWS}$		18.0		20.1		22.7	ns
$t_{LEPERIPH}$		8.1		8.6		9.5	ns
$t_{LABCARRY}$		0.6		0.8		1.0	ns
$t_{LABCASC}$		0.8		1.0		1.2	ns

EPF10K130V Device External Timing Parameters *Notes (1), (2)*							
Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{DRR}		15.0		19.1		24.2	ns
t_{INSU}, *Notes (3), (4)*	6.9		8.6		11.0		ns
t_{INH}, *Note (4)*	0.0		0.0		0.0		ns
t_{OUTCO}, *Note (4)*		7.8		9.9		11.3	ns
t_{ODH}, *Note (4)*	2.0		2.0		2.0		ns

Notes to tables:

(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.
(3) Using an LE to register the signal may provide a lower setup time.
(4) This parameter is specified by characterization.

EPF10K100A Device Internal & External Timing Parameters

EPF10K100A Device LE Timing Microparameters *Notes (1), (2)*							
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{LUT}		1.0		1.2		1.4	ns
t_{CLUT}		0.8		0.9		1.1	ns
t_{RLUT}		1.4		1.6		1.9	ns
t_{PACKED}		0.4		0.5		0.5	ns
t_{EN}		0.6		0.7		0.8	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		0.4		0.4		0.6	ns
t_{CGENR}		0.6		0.7		0.8	ns
t_{CASC}		0.7		0.9		1.0	ns
t_{C}		0.9		1.0		1.2	ns
t_{CO}		0.2		0.3		0.3	ns
t_{COMB}		0.6		0.7		0.8	ns
t_{SU}	0.8		1.0		1.2		ns
t_{H}	0.3		0.5		0.5		ns
t_{PRE}		0.3		0.3		0.4	ns
t_{CLR}		0.3		0.3		0.4	ns
t_{CH}	2.5		3.5		3.5		ns
t_{CL}	2.5		3.5		3.5		ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.

EPF10K100A Device IOE Timing Microparameters *Notes (1), (2)*							
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		2.5		2.9		3.4	ns
t_{IOC}		0.3		0.3		0.4	ns
t_{IOCO}		0.2		0.2		0.3	ns
t_{IOCOMB}		0.5		0.6		0.7	ns
t_{IOSU}	1.3		1.7		1.8		ns
t_{IOH}	0.2		0.2		0.3		ns
t_{IOCLR}		1.0		1.2		1.4	ns
t_{OD1}		2.2		2.6		3.0	ns
t_{OD2}		4.5		5.3		6.1	ns
t_{OD3}		6.8		7.9		9.3	ns
t_{XZ}		2.7		3.1		3.7	ns
t_{ZX1}		2.7		3.1		3.7	ns
t_{ZX2}		5.0		5.8		6.8	ns
t_{ZX3}		7.3		8.4		10.0	ns
t_{INREG}		5.3		6.1		7.2	ns
t_{IOFD}		4.7		5.5		6.4	ns
t_{INCOMB}		4.7		5.5		6.4	ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.

EPF10K100A Device EAB Internal Microparameters *Notes (1), (2)*							
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{EABDATA1}$		1.8		2.1		2.4	ns
$t_{EABDATA2}$		3.2		3.7		4.4	ns
t_{EABWE1}		0.8		0.9		1.1	ns
t_{EABWE2}		2.3		2.7		3.1	ns
t_{EABCLK}		0.8		0.9		1.1	ns
t_{EABCO}		1.0		1.1		1.4	ns
$t_{EABBYPASS}$		0.3		0.3		0.4	ns
t_{EABSU}	1.3		1.5		1.8		ns
t_{EABH}	0.4		0.5		0.5		ns
t_{AA}		4.1		4.8		5.6	ns
t_{WP}	3.2		3.7		4.4		ns
t_{WDSU}	2.4		2.8		3.3		ns
t_{WDH}	0.2		0.2		0.3		ns
t_{WASU}	0.2		0.2		0.3		ns
t_{WAH}	0.0		0.0		0.0		ns
t_{WO}		3.4		3.9		4.6	ns
t_{DD}		3.4		3.9		4.6	ns
t_{EABOUT}		0.3		0.3		0.4	ns
t_{EABCH}	2.5		3.5		4.0		ns
t_{EABCL}	4.0		4.0		4.0		ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.

EPF10K100A Device EAB Internal Timing Macroparameters *Notes (1), (2)*							
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		6.8		7.8		9.2	ns
$t_{EABRCCOMB}$	6.8		7.8		9.2		ns
$t_{EABRCREG}$	5.4		6.2		7.4		ns
t_{EABWP}	3.2		3.7		4.4		ns
$t_{EABWCCOMB}$	3.4		3.9		4.7		ns
$t_{EABWCREG}$	9.4		10.8		12.8		ns
t_{EABDD}		6.1		6.9		8.2	ns
$t_{EABDATACO}$		2.1		2.3		2.9	ns
$t_{EABDATASU}$	3.7		4.3		5.1		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	2.8		3.3		3.8		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	3.4		4.0		4.6		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	1.9		2.3		2.6		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		5.1		5.7		6.9	ns

Notes:
(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.

EPF10K100A Device Interconnect Timing Microparameters *Notes (1), (2)*							
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		4.8		5.4		6.0	ns
t_{DIN2LE}		2.0		2.4		2.7	ns
$t_{DIN2DATA}$		2.4		2.7		2.9	ns
$t_{DCLK2IOE}$		2.6		3.0		3.5	ns
$t_{DCLK2LE}$		2.0		2.4		2.7	ns
$t_{SAMELAB}$		0.1		0.1		0.1	ns
$t_{SAMEROW}$		1.5		1.7		1.9	ns
$t_{SAMECOLUMN}$		5.5		6.5		7.4	ns
$t_{DIFFROW}$		7.0		8.2		9.3	ns
$t_{TWOROWS}$		8.5		9.9		11.2	ns
$t_{LEPERIPH}$		3.9		4.2		4.5	ns
$t_{LABCARRY}$		0.2		0.2		0.3	ns
$t_{LABCASC}$		0.4		0.5		0.6	ns

EPF10K100A Device External Timing Parameters *Notes (1), (2)*							
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{DRR}		12.5		14.5		17.0	ns
t_{INSU}, *Notes (3), (4)*	3.7		4.5		5.1		ns
t_{INH}, *Note (4)*	0.0		0.0		0.0		ns
t_{OUTCO}, *Note (4)*		5.3		6.1		7.2	ns
t_{ODH}, *Note (4)*	2.0		2.0		2.0		ns

Notes to tables:

(1) All timing parameters are described in Tables 14 through 20 in this data sheet.
(2) These parameters are preliminary. For the most up-to-date information, contact Altera Applications.
(3) Using an LE to register the signal may provide a lower setup time.
(4) This parameter is specified by characterization.

External Reference Timing Parameters *Note (1)*								
Symbol	**Device**	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		**Unit**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{DRR}	EPF10K10A		10.0		12.0		16.0	ns
	EPF10K30A		11.0		14.0		17.0	ns
	EPF10K100B		10.5		12.0		13.5	ns
	EPF10K250A		14.5		16.5		19.0	ns

Note:
(1) These timing parameters are preliminary. For the most up-to-date information, contact Altera Applications at (800) 800-EPLD.

ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. Figure 28 illustrates the incoming and generated clock specifications.

Figure 28. Specifications for the Incoming & Generated Clocks

The t_I parameter refers to the nominal input clock period; the t_O parameter refers to the nominal output clock period.

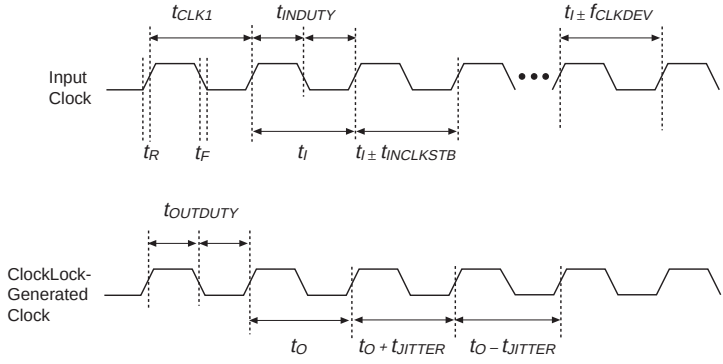


Table 21 summarizes the ClockLock and ClockBoost parameters.

Table 21. ClockLock & ClockBoost Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_R	Input rise time			2	ns
t_F	Input fall time			2	ns
t_{INDUTY}	Input duty cycle	45		55	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)	30		80	MHz
t_{CLK1}	Input clock period (ClockBoost clock multiplication factor equals 1)	12.5		33.3	ns
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	16		50	MHz
t_{CLK2}	Input clock period (ClockBoost clock multiplication factor equals 2)	20		62.5	ns
$f_{CLKDEV1}$	Input deviation from user specification in MAX+PLUS II, (ClockBoost clock multiplication factor equals 1), *Note (1)*			±1	MHz
$f_{CLKDEV2}$	Input deviation from user specification in MAX+PLUS II, (ClockBoost clock multiplication factor equals 2), *Note (1)*			±0.5	MHz
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)			100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock, *Note (2)*			10	µs
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock, *Note (3)*			1	ns
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock	40	50	60	%

Notes:

(1) To implement the ClockLock and ClockBoost circuitry with the MAX+PLUS II software, designers must specify the input frequency. The MAX+PLUS II software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The f_{CLKDEV} parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.

(2) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the t_{LOCK} value is less than the time required for configuration.

(3) The t_{JITTER} specification is measured under long-term observation.

Power Consumption

The supply power (P) for FLEX 10K devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

Typical $I_{CCSTANDBY}$ values are shown as I_{CC0} in the "FLEX 10K 5.0-V Device DC Operating Conditions" table on pages 41, 44, and 46 of this data sheet. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value is calculated based on the amount of current that each LE typically consumes. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)* in this data book.

Compared to the rest of the device, the embedded array consumes a negligible amount of power. Therefore, the embedded array can be ignored when calculating supply current.

The $I_{CCACTIVE}$ value is calculated with the following equation:

$$I_{CCACTIVE} = K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}} \times \frac{\mu A}{MHz \times LE}$$

The parameters in this equation are shown below:

$\mathbf{f_{MAX}}$ = Maximum operating frequency in MHz
N = Total number of logic cells used in the device
$\mathbf{tog_{LC}}$ = Average percent of logic cells toggling at each clock (typically 12.5%)
K = Constant, shown in Table 22

Table 22. K Constant Values

Device	K Value
EPF10K10	82
EPF10K20	89
EPF10K30	88
EPF10K40	92
EPF10K50	95
EPF10K70	85
EPF10K100	88
EPF10K10A	25, *Note (1)*
EPF10K30A	23, *Note (1)*
EPF10K50V	45
EPF10K130V	29
EPF10K100A	29, *Note (1)*
EPF10K100B	19, *Note (1)*
EPF10K250A	42, *Note (1)*

Note:
(1) This value is preliminary. For the most up-to-date information, contact Altera Applications.

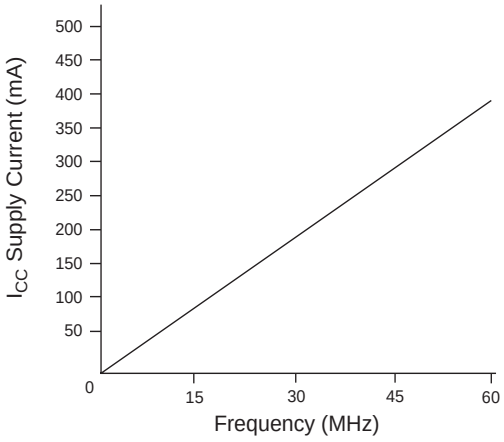
This calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

In order to better reflect actual designs, the power model (and the constant *K* in the power calculation equations shown above) for continuous interconnect FLEX devices assumes that logic cells drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assumes that all logic cells drive only one short interconnect segment. This assumption may lead to inaccurate results, compared to measured power consumption for an actual design in a segmented interconnect FPGA.

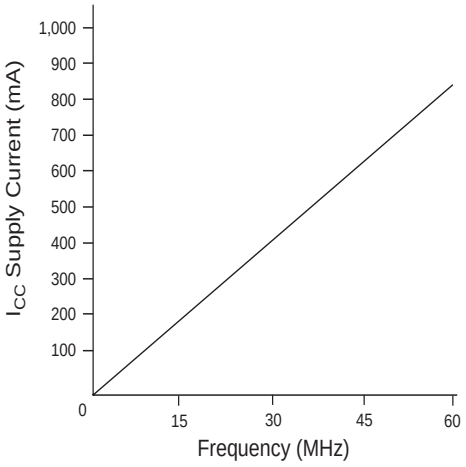
Figure 29 shows the relationship between the current and operating frequency of FLEX 10K devices. For other FLEX 10KA devices, contact Altera Applications.

Figure 29. $I_{CCACTIVE}$ vs. Operating Frequency (Part 1 of 4) *Note (1)*

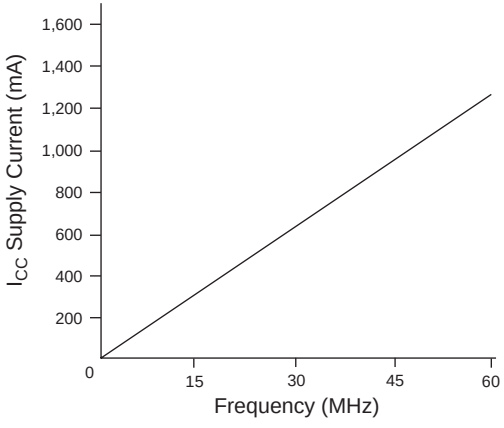
EPF10K10



EPF10K20



EPF10K30



EPF10K30A

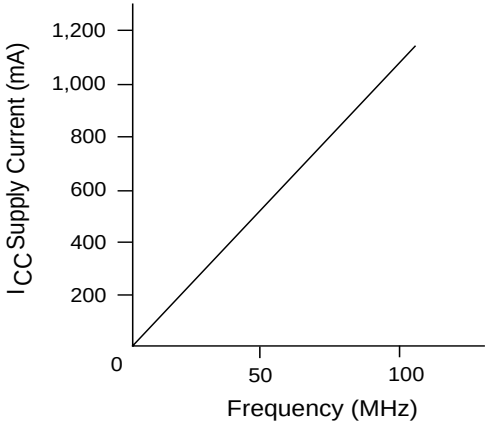
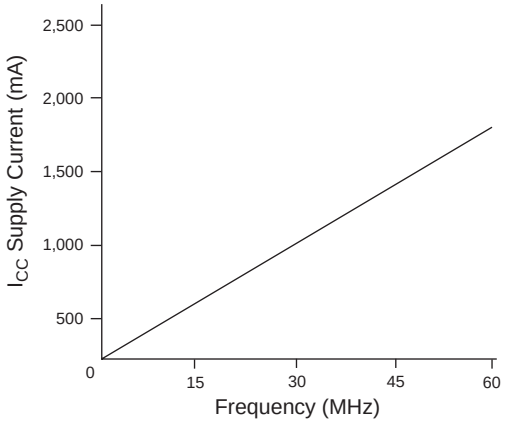
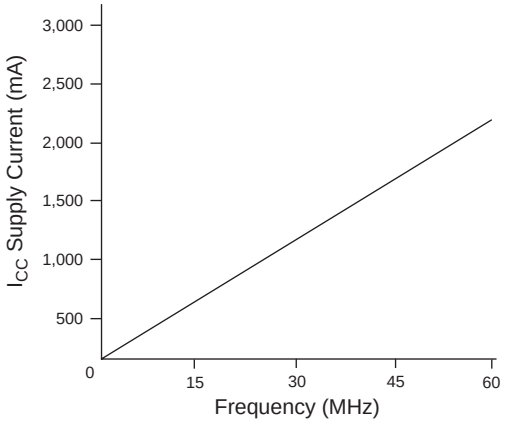


Figure 29. $I_{CCACTIVE}$ vs. Operating Frequency (Part 2 of 4) *Note (1)*

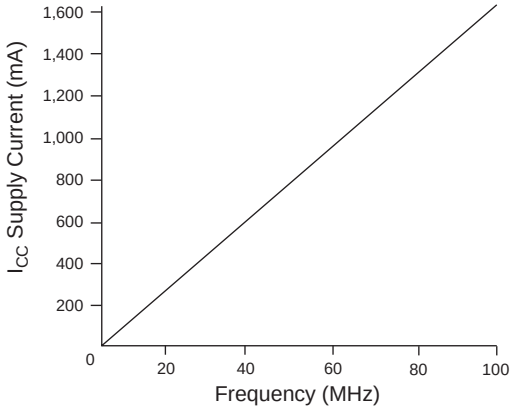
EPF10K40



EPF10K50



EPF10K50V



EPF10K70

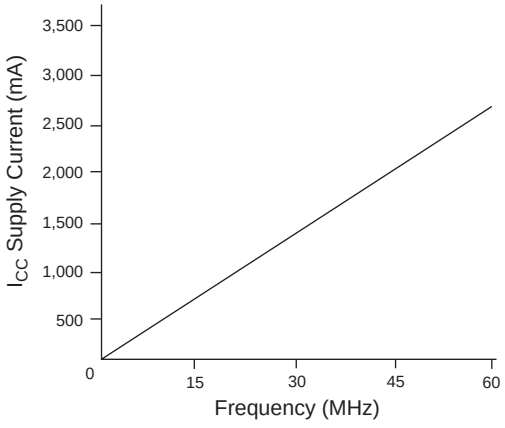
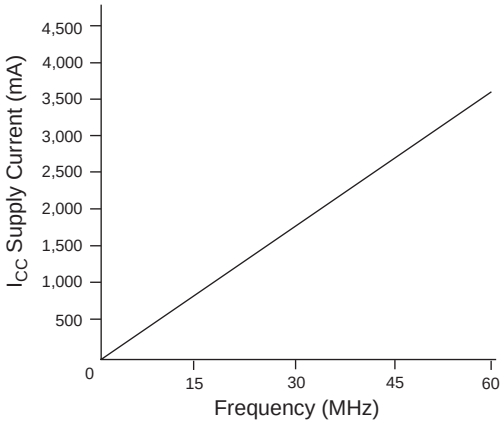
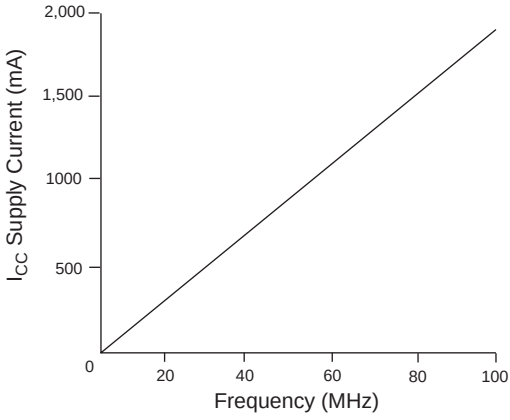


Figure 29. $I_{CCACTIVE}$ vs. Operating Frequency (Part 3 of 4) *Note (1)*

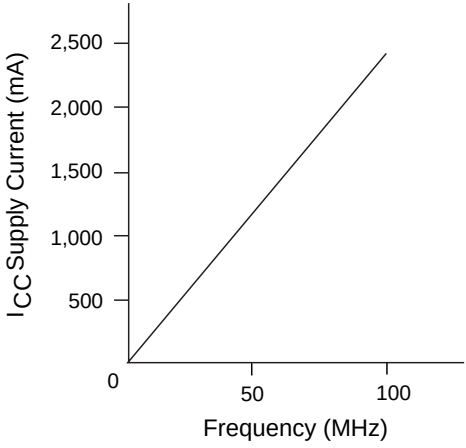
EPF10K100



EPF10K100A



EPF10K100B



EPF10K130V

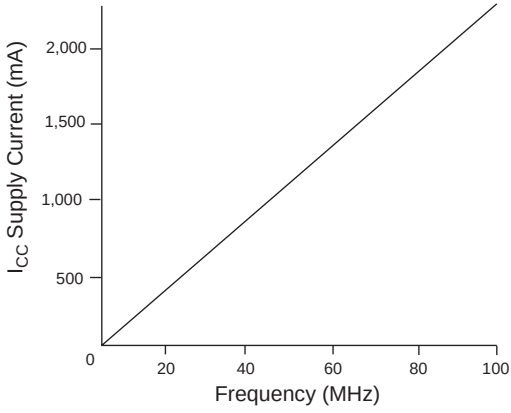
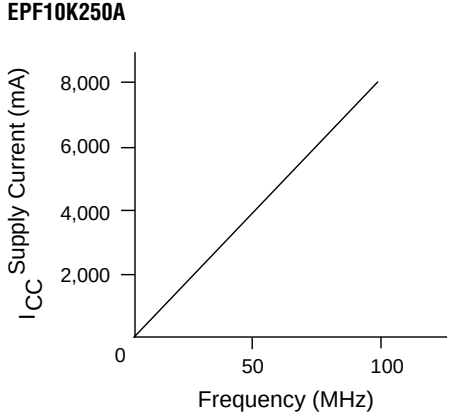


Figure 29. $I_{CCACTIVE}$ vs. Operating Frequency (Part 4 of 4) *Note (1)*



Note:
(1) The information on EPF10K30A, EPF10K100B, and EPF10K250A devices are preliminary. Contact Altera Applications at (800) 800-EPLD for the most up-to-date information

Configuration & Operation

The FLEX 10K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Go to *AN 59 (Configuring FLEX 10K Devices)* for detailed descriptions of device configuration options; device configuration pins; and information on configuring FLEX 10K devices, including sample schematics, timing diagrams, and configuration parameters.

Operating Modes

The FLEX 10K architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. The process of physically loading the SRAM data into the device is called *configuration*. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow FLEX 10K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 320 ms and can be used to reconfigure an entire system dynamically. In-field upgrades can be performed by distributing new configuration files.

Programming Files

Despite being function- and pin- compatible, FLEX 10KA and FLEX 10KE devices are not programming- or configuration-file compatible with FLEX 10K devices. A design should be recompiled before it is transferred from a FLEX 10K device to an equivalent FLEX 10KA or FLEX 10KE device. This recompilation should be performed to create a new programming or configuration file and to check design timing on the faster FLEX 10KA or FLEX 10KE device. Although the programming or configuration files for the EPF10K50 device can program or configure a EPF10K50V device, Altera recommends recompiling a design with the EPF10K50V device when transferring a design from the EPF10K50 device.

Configuration Schemes

The configuration data for a FLEX 10K device can be loaded with one of five configuration schemes (see Table 23), chosen on the basis of the target application. An EPC1 or EPC1441 Configuration EPROM, intelligent controller, or the JTAG port can be used to control the configuration of a FLEX 10K device, allowing automatic configuration on system power-up.

Multiple FLEX 10K devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 23. Data Sources for Configuration

Configuration Scheme	Data Source
Configuration EPROM	EPC1 or EPC1441 Configuration EPROM
Passive serial (PS)	BitBlaster, ByteBlaster, or ByteBlasterMV download cable, or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	BitBlaster, ByteBlaster, or ByteBlasterMV download cable, or microprocessor with Jam File

Device Pin-Outs

Tables 24 through 26 show the pin names and numbers for the dedicated pins in each FLEX 10K device package.

Table 24. FLEX 10K Device Pin-Outs (Part 1 of 3) *Notes (1), (2)*

Pin Name	84-Pin PLCC EPF10K10	144-Pin TQFP EPF10K10 EPF10K10A EPF10K20 EPF10K30A	208-Pin PQFP EPF10K10 EPF10K10A	208-Pin PQFP/ RQFP EPF10K20 EPF10K30 EPF10K30A EPF10K40	240-Pin PQFP/RQFP EPF10K20 EPF10K30 EPF10K40 EPF10K50 EPF10K50V EPF10K70	240-Pin PQFP/RQFP EPF10K30A EPF10K100A
MSEL0 *(3)*	31	77	108	108	124	124
MSEL1 *(3)*	32	76	107	107	123	123
nSTATUS *(3)*	55	35	52	52	60	60
nCONFIG *(3)*	34	74	105	105	121	121
DCLK *(3)*	13	107	155	155	179	179
CONF_DONE *(3)*	76	2	2	2	2	2
INIT_DONE *(4)*	69	14	19	19	26	26
nCE *(3)*	14	106	154	154	178	178
nCEO *(3)*	75	3	3	3	3	3
nWS *(5)*	80	142	206	206	238	238
nRS *(5)*	81	141	204	204	236	236
nCS *(5)*	78	144	208	208	240	240
CS *(5)*	79	143	207	207	239	239
RDYnBSY *(5)*	70	11	16	16	23	23
CLKUSR *(5)*	73	7	10	10	11	11
DATA7 *(5)*	5	116	166	166	190	190
DATA6 *(5)*	6	114	164	164	188	188
DATA5 *(5)*	7	113	162	162	186	186
DATA4 *(5)*	8	112	161	161	185	185
DATA3 *(5)*	9	111	159	159	183	183
DATA2 *(5)*	10	110	158	158	182	182
DATA1 *(5)*	11	109	157	157	181	181
DATA0 *(3)*, *(6)*	12	108	156	156	180	180
TDI *(3)*	15	105	153	153	177	177
TDO *(3)*	74	4	4	4	4	4
TCK *(3)*	77	1	1	1	1	1
TMS *(3)*	57	34	50	50	58	58

Table 24. FLEX 10K Device Pin-Outs (Part 2 of 3) *Notes (1), (2)*

Pin Name	84-Pin PLCC EPF10K10	144-Pin TQFP EPF10K10 EPF10K10A EPF10K20 EPF10K30A	208-Pin PQFP EPF10K10 EPF10K10A	208-Pin PQFP/ RQFP EPF10K20 EPF10K30 EPF10K30A EPF10K40	240-Pin PQFP/RQFP EPF10K20 EPF10K30 EPF10K40 EPF10K50 EPF10K50V EPF10K70	240-Pin PQFP/RQFP EPF10K30A EPF10K100A
TRST *(3)*	56	*Note (7)*	51	51	59	59
Dedicated Inputs	2, 42, 44, 84	54, 56, 124, 126	78, 80, 182, 184	78, 80, 182, 184	90, 92, 210, 212	90, 92, 210, 212
Dedicated Clock Pins	1, 43	55, 125	79, 183	79, 183	91, 211	91, 211
DEV_CLRn *(4)*	3	122	180	180	209	209
DEV_OE *(4)*	83	128	186	186	213	213
VCCINT	4, 20, 33, 40, 45, 63	6, 25, 52, 53, 75, 93, 123	6, 23, 35, 43, 76, 77, 106, 109, 117, 137, 145, 181	6, 23, 35, 43, 76, 77, 106, 109, 117, 137, 145, 181	5, 16, 27, 37, 47, 57, 77, 89, 96, 112, 122, 130, 140, 150, 160, 170, 189, 205, 224	5, 27, 47, 89, 96, 122, 130, 150, 170
VCCIO	–	5, 24, 45, 61, 71, 94, 115, 134	5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194	5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194	–	16, 37, 57, 77, 112, 140, 160, 189, 205, 224
GNDINT	26, 41, 46, 68, 82	16, 57, 58, 84, 103, 127	21, 33, 49, 81, 82, 123, 129, 151, 185	21, 33, 49, 81, 82, 123, 129, 151, 185	10, 22, 32, 42, 52, 69, 85, 93, 104, 125, 135, 145, 155, 165, 176, 197, 216, 232	10, 22, 32, 42, 52, 69, 85, 93, 104, 125, 135, 145, 155, 165, 176, 197, 216, 232
GNDIO	–	15, 40, 50, 66, 85, 104, 129, 139	20, 32, 48, 59, 72, 91, 124, 130, 152, 171, 188, 201	20, 32, 48, 59, 72, 91, 124, 130, 152, 171, 188, 201	–	–

Table 24. FLEX 10K Device Pin-Outs (Part 3 of 3) *Notes (1), (2)*

Pin Name	84-Pin PLCC EPF10K10	144-Pin TQFP EPF10K10 EPF10K10A EPF10K20 EPF10K30A	208-Pin PQFP EPF10K10 EPF10K10A	208-Pin PQFP/ RQFP EPF10K20 EPF10K30 EPF10K30A EPF10K40	240-Pin PQFP/RQFP EPF10K20 EPF10K30 EPF10K40 EPF10K50 EPF10K50V EPF10K70	240-Pin PQFP/RQFP EPF10K30A EPF10K100A
No Connect (N.C.) *(8)*	–	–	7, 8, 9, 14, 15, 36, 37, 113, 114, 125, 126, 139, 140	–	–	–
Total User I/O Pins *(9)*	59	102	134	147	189	189

Table 25. FLEX 10K Pin-Outs (Part 1 of 3) *Notes (1), (2)*

Pin Name	356-Pin BGA EPF10K30 EPF10K30A	356-Pin BGA EPF10K50 EPF10K50V EPF10K100A	403-Pin PGA EPF10K50	503-Pin PGA EPF10K70
MSEL0 *(3)*	D4	D4	AN1	AT40
MSEL1 *(3)*	D3	D3	AR1	AV40
nSTATUS *(3)*	D24	D24	AU37	AY4
nCONFIG *(3)*	D2	D2	AU1	AY40
DCLK *(3)*	AC5	AC5	E1	H40
CONF_DONE *(3)*	AC24	AC24	C37	F4
INIT_DONE *(4)*	T24	T24	R35	V6
nCE *(3)*	AC2	AC2	G1	K40
nCEO *(3)*	AC22	AC22	E37	H4
nWS *(5)*	AE24	AE24	E31	A3
nRS *(5)*	AE23	AE23	A33	C5
nCS *(5)*	AD24	AD24	A35	C1
CS *(5)*	AD23	AD23	C33	C3
RDYnBSY *(5)*	U22	U22	N35	T6
CLKUSR *(5)*	AA24	AA24	G35	H6
DATA7 *(5)*	AF4	AF4	C9	E29
DATA6 *(5)*	AD8	AD8	A7	D30
DATA5 *(5)*	AE5	AE5	E9	C31
DATA4 *(5)*	AD6	AD6	C7	B32
DATA3 *(5)*	AF2	AF2	A5	D32
DATA2 *(5)*	AD5	AD5	E7	B34
DATA1 *(5)*	AD4	AD4	C5	E33
DATA0 *(3)*, *(6)*	AD3	AD3	C1	F40
TDI *(3)*	AC3	AC3	J1	M40
TDO *(3)*	AC23	AC23	G37	K4
TCK *(3)*	AD25	AD25	A37	D4
TMS *(3)*	D22	D22	AN37	AT4
TRST *(3)*	D23	D23	AR37	AV4
Dedicated Inputs	A13, B14, AF14, AE13,	A13, B14, AF14, AE13	A17, A21, AU17, AU21	D20, D24, AY24, AY20
Dedicated Clock Pins	A14, AF13	A14, AF13	A19, AU19	D22, AY22
DEV_CLRn *(4)*	AD13	AD13	C17	F22
DEV_OE *(4)*	AE14	AE14	C19	G21

Table 25. FLEX 10K Pin-Outs (Part 2 of 3) *Notes (1), (2)*

Pin Name	356-Pin BGA EPF10K30 EPF10K30A	356-Pin BGA EPF10K50 EPF10K50V EPF10K100A	403-Pin PGA EPF10K50	503-Pin PGA EPF10K70
VCCINT	A1, A26, C14, C26, D5, F1, H22, J1, M26, N1, T26, U5, AA1, AD26, AF1, AF26	A1, A26, C14, C26, D5, F1, H22, J1, M26, N1, T26, U5, AA1, AD26, AF1, AF26	B2, D14, E25, F22, K36, T2, T32, V6, AD34, AE5, AL5, AM6, AM20, AN25, AN29, AP4, AT16, AT36	C11, E39, G27, N5, N41, W39, AC3, AG7, AR3, AR41, AU37, AW5, AW25, AW41, BA17, BA19
VCCIO	A7, A23, B4, C15, D25, F4, H24, K5, M23, P2, T25, V2, W22, AB1, AC25, AD18, AF3, AF7, AF16	A7, A23, B4, C15, D25, F4, H24, K5, M23, P2, T25, V2, W22, AB1, AC25, AD18, AF3, AF7, AF16	B22, D34, E11, E27, F16, L5, L33, P4, T6, T36, V32, AB36, AG5, AG33, AH2, AM18, AM32, AN11, AN27, AP24, AT22	C9, C15, C25, C33, C37, E19, E41, G7, L3, R41, U3, U37, W5, AC41, AE5, AJ41, AL39, AU3, AU17, AW3, AW19, BA9, BA27, BA29, BA37
GNDINT	A2, A10, A20, B1, B13, B22, B25, B26, C2, C9, C13, C25, H23, J26, K1, M1, N26, R1, R26, T1, U26, W1, AD2, AD14, AD20, AE1, AE2, AE7, AE25, AE26, AF11, AF19, AF25	A2, A10, A20, B1, B13, B22, B25, B26, C2, C9, C13, C25, H23, J26, K1, M1, N26, R1, R26, T1, U26, W1, AD2, AD14, AD20, AE1, AE2, AE7, AE25, AE26, AF11, AF19, AF25	B16, B36, D4, E21, F18, F32, G33, P34, U5, Y32, AA33, AB2, AB6, AH36, AM16, AN17, AN21, AP14, AT2	C17, E3, E5, E25, G37, J3, J41, U7, AA3, AE39, AL5, AL41, AU27, AW39, BA7, BA13, BA25
GNDIO	–	–	B10, B28, D24, E5, E19, E33, F6, F20, K2, W5, W33, Y6, AB32, AD4, AM22, AN5, AN19, AN33, AP34, AT10, AT28	C21, C23, C39, C41, E13, E31, G3, G17, N3, N39, R3, W41, W3, AA41, AG37, AJ3, AN3, AN41, AU7, AU41, AW13, AW31, BA11, BA21, BA23

Table 25. FLEX 10K Pin-Outs (Part 3 of 3) *Notes (1), (2)*

Pin Name	356-Pin BGA EPF10K30 EPF10K30A	356-Pin BGA EPF10K50 EPF10K50V EPF10K100A	403-Pin PGA EPF10K50	503-Pin PGA EPF10K70
No Connect (N.C.) *(10)*, *(11)*	C1, D1, D26, E1, E2, G1, G5, G23, G26, H1, H25, H26, J25, K25, P24, R24, T23, U25, V1, V3, V4, V26, W2, W3, Y1, Y2, Y23, AC26	–	–	A19, A21, A23, A31, A33, A35, A39, A41, B16, B18, B22, B24, B30, B40, C29, C35, D18, D26, D28, D38, E27, E37, F18, F2, F26, F30, F32, G23, G25, G29, G31, G33, G35, K6, K42, L39, L43, M2, N7, P38, P4, P42, R37, T40, V42, AC5, AD2, AE3
Total User I/O Pins *(9)*	246	274	310	358

Table 26. FLEX 10K Pin-Outs (Part 1 of 3) *Notes (1), (2)*

Pin Name	503-Pin PGA EPF10K100	599-Pin PGA EPF10K130V EPF10K250A	600-Pin BGA EPF10K100A	600-Pin BGA EPF10K130V EPF10K250A
MSEL0 *(3)*	AT40	F6	F5	F5
MSEL1 *(3)*	AV40	C3	C1	C1
nSTATUS *(3)*	AY4	E43	D32	D32
nCONFIG *(3)*	AY40	B4	D4	D4
DCLK *(3)*	H40	BE5	AP1	AP1
CONF_DONE *(3)*	F4	BC43	AM32	AM32
INIT_DONE *(4)*	V6	AM40	AE32	AE32
nCE *(3)*	K40	BB6	AN2	AN2
nCEO *(3)*	H4	BF44	AP35	AP35
nWS *(5)*	A3	BB40	AR29	AR29
nRS *(5)*	C5	BA37	AM28	AM28
nCS *(5)*	C1	AY38	AL29	AL29
CS *(5)*	C3	BA39	AN29	AN29
RDYnBSY *(5)*	T6	AW47	AG35	AG35
CLKUSR *(5)*	H6	AY42	AM34	AM34
DATA7 *(5)*	E29	BD14	AM13	AM13
DATA6 *(5)*	D30	BA17	AR12	AR12
DATA5 *(5)*	C31	BB16	AN12	AN12
DATA4 *(5)*	B32	BF12	AP11	AP11
DATA3 *(5)*	D32	BG11	AM11	AM11
DATA2 *(5)*	B34	BG9	AR10	AR10
DATA1 *(5)*	E33	BF10	AN10	AN10
DATA0 *(3)*, *(6)*	F40	BC5	AM4	AM4
TDI *(3)*	M40	BF4	AN1	AN1
TDO *(3)*	K4	BB42	AN34	AN34
TCK *(3)*	D4	BE43	AL31	AL31
TMS *(3)*	AT4	F42	C35	C35
TRST *(3)*	AV4	B46	C34	C34
Dedicated Inputs	D20, D24, AY24, AY20	B24, C25, BG25, BG23	C18, D18, AM18, AN18	C18, D18, AM18, AN18
Dedicated Clock Pins	D22, AY22	BF24, A25	AL18, E18	AL18, E18
LOCK *(12)*	AV14	–	–	–
GCLK1 *(13)*	AY22	–	–	–
DEV_CLRn *(4)*	F22	BE23	AR17	AR17

Table 26. FLEX 10K Pin-Outs (Part 2 of 3) *Notes (1), (2)*

Pin Name	503-Pin PGA EPF10K100	599-Pin PGA EPF10K130V EPF10K250A	600-Pin BGA EPF10K100A	600-Pin BGA EPF10K130V EPF10K250A
DEV_OE *(4)*	G21	BC25	AR19	AR19
VCCINT	C11, E39, G27, N5, N41, W39, AC3, AG7, AR3, AR41, AU37, AW5, AW25, AW41, BA17, BA19	E5, A3, A45, C1, C11, C19, C29, C37, C47, G25, L3, L45, W3, W45, AJ3, AJ45, AU3, AU45, BE1, BE11, BE19, BE29, BE37, BE47, BG3, BG45	AL3, AG5, AE4, AB5, Y2, U3, P5, M2, H1, B1, A11, B18, D24, F31, F35, K32, N34, T35, V32, AA33, AD35, AF32, AK35, AK31, AP24, AR18, AR11, E2, A19	AL3, AG5, AE4, AB5, Y2, U3, P5, M2, H1, B1, A11, B18, D24, F31, F35, K32, N34, T35, V32, AA33, AD35, AF32, AK35, AK31, AP24, AR18, AR11, E2, A19
VCCIO	C9, C15, C25, C33, C37, E19, E41, G7, L3, R41, U3, U37, W5, AC41, AE5, AJ41, AL39, AU3, AU17, AW3, AW19, BA9, BA27, BA29, BA37	D24, E9, E15, E21, E27, E33, E39, G7, G41, J5, J43, R5, R43, AA5, AA43, AD4, AD44, AG5, AG43, AN5, AN43, AW5, AW43, BA7, BA41, BC9, BC15, BC21, BC27, BC33, BC39, BD24	C8, E12, C15, A20, C23, A27, AM26, AR23, AM19, AN15, AL12, AN8, C2, C3, C4, D5, E5, C33, C32, D31, E31, AL5, AM5, AN4, AN3, AM31, AN32, AN33, AP34	C8, E12, C15, A20, C23, A27, AM26, AR23, AM19, AN15, AL12, AN8, C2, C3, C4, D5, E5, C33, C32, D31, E31, AL5, AM5, AN4, AN3, AM31, AN32, AN33, AP34
VCC_CKLK *(15)*	BA19	–	–	–
GNDINT	C17, E3, E5, E25, G37, J3, J41, U7, AA3, AE39, AL5, AL41, AU27, AW39, BA7, BA13, BA25	A47, B2, C13, C21, C27, C35, C45, D4, G23, N3, N45, AA3, AA45, AG3, AG45, AR3, AR45, BD44, BE3, BE13, BE21, BE27, BE35, BE45, BG1, BG47	A18, AN35, A1, A2, A3, A4, A5, B2, B3, B4, B5, B6, C5, C6, D6, E6, A31, A32, A33, A34, A35, B31, B32, B33, B34, B35, C30, C31, D30	A18, AN35, A1, A2, A3, A4, A5, B2, B3, B4, B5, B6, C5, C6, D6, E6, A31, A32, A33, A34, A35, B31, B32, B33, B34, B35, C30, C31, D30
GNDIO	C21, C23, C39, C41, E13, E31, G3, G17, N3, N39, R3, W3, W41, AA41, AG37, AJ3, AN3, AN41, AU7, AU41, AW13, AW31, BA11, BA23, BA21	E7, E13, E19, E29, E35, E41, F24, G5, G43, H40, N5, W5, W43, AD6, AD42, AJ5, AJ43, AR5, AR43, AY8, AY40, BA5, BA43, BB24, BC7, BC13, BC19, BC29, BC35, BC41, N43	E30, AL6, AM6, AN5, AN6, AP2, AP3, AP4, AP5, AP6, AR1, AR2, AR3, AR4, AR5, AL30, AM30, AN30, AN31, AP30, AP31, AP32, AP33, AR30, AR31, AR32, AR33, AR34, AR35	E30, AL6, AM6, AN5, AN6, AP2, AP3, AP4, AP5, AP6, AR1, AR2, AR3, AR4, AR5, AL30, AM30, AN30, AN31, AP30, AP31, AP32, AP33, AR30, AR31, AR32, AR33, AR34, AR35
VGND_CKLK *(15)*	BA25	–	–	–

Table 26. FLEX 10K Pin-Outs (Part 3 of 3) *Notes (1), (2)*

Pin Name	503-Pin PGA EPF10K100	599-Pin PGA EPF10K130V EPF10K250A	600-Pin BGA EPF10K100A	600-Pin BGA EPF10K130V EPF10K250A
No Connect (N.C.) *(14)*	–	–	AK5, AL4, AM3, AM2, AM1, AJ5, AL2, AK4, AL1, AK3, AJ4, AH5, AK2, AK1, AJ3, AJ2, G1, G2, G3, F1, F2, H5, G4, F3, E1, E3, F4, G5, D1, D2, D3, E4, E32, D33, D34, D35, G31, F32, E33, E34, E35, F33, G32, H31, F34, G33, G34, G35, AB34, AB33, AB32, AB31, AC35, AC34, AC33, AC32, AC31, AD34, AD33, AD32, AD31, AE35, AE34, AE33	–
Total User I/O Pins *(9)*	406	470	406	470

Notes to tables:

(1) All pins that are not listed are user I/O pins.
(2) Pin-out information on FLEX 10KA devices (except EPF10K50V, EPF10K130V, and EPF10K100A devices) and FLEX 10KB devices are preliminary. Contact Altera Applications for the latest pin-out information.
(3) This pin is a dedicated pin; it is not available as a user I/O pin.
(4) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(5) This pin can be used as a user I/O pin after configuration.
(6) This pin is tri-stated in user mode.
(7) The optional JTAG pin TRST is not used in the 144-pin TQFP package.
(8) To maintain pin compatibility when transferring to the EPF10K10 device from any other device in the 208-pin PQFP package, do not use these pins as user I/O pins.
(9) The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.
(10) To maintain pin compatibility when transferring to the EPF10K30 device from any other device in the 356-pin BGA package, do not use these pins as user I/O pins.
(11) To maintain pin compatibility when transferring from the EPF10K100 to the EPF10K70 in the 503-pin PGA package, do not use these pins as user I/O pins.
(12) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(13) This pin drives the ClockLock and ClockBoost circuitry.
(14) To maintain pin compatibility when transferring a to the EPF10K100A device from another device in the 600-pin BGA package, do not use these pin as user I/O pins.
(15) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device.

Revision History

The information contained in the *FLEX 10K Embedded Programmable Logic Family Data Sheet* version 3.11 supersedes information published in previous versions.

Version 3.11 Changes

The *FLEX 10K Embedded Programmable Logic Family Data Sheet* version 3.11 contains the following changes:

- Added the EPF10K30A device to the 356-pin BGA column of Table 4.
- Added information on using input pins as internally generated global signals to page 31.
- Added the EPF10K30A device to the 356-pin BGA column of Table 25.

Version 3.10 Changes

The *FLEX 10K Embedded Programmable Logic Family Data Sheet* version 3.10 contained the following changes:

- Deleted all references to FLEX 10KB devices.
- Added information on the PCI clamping diode.
- Added information on the ByteBlasterMV parallel port download cable.
- Revised timing information for EPF10K50V, EPF10K70, and EPF10K100A devices.
- Updated K constant values in the "Power Consumption" section.
- Added $I_{CCACTIVE}$ vs. Operating Frequency graphs for EPF10K30A, EPF10K100B, and EPF10K250A devices in Figure 29.
- Updated the "MultiVolt I/O Interface" section.
- Revised the `VCCINT` and `VCCIO` pins of the 240-pin PQFO/RQFP package for EPF10K30A and EPF10K100A devices in Table 24.

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