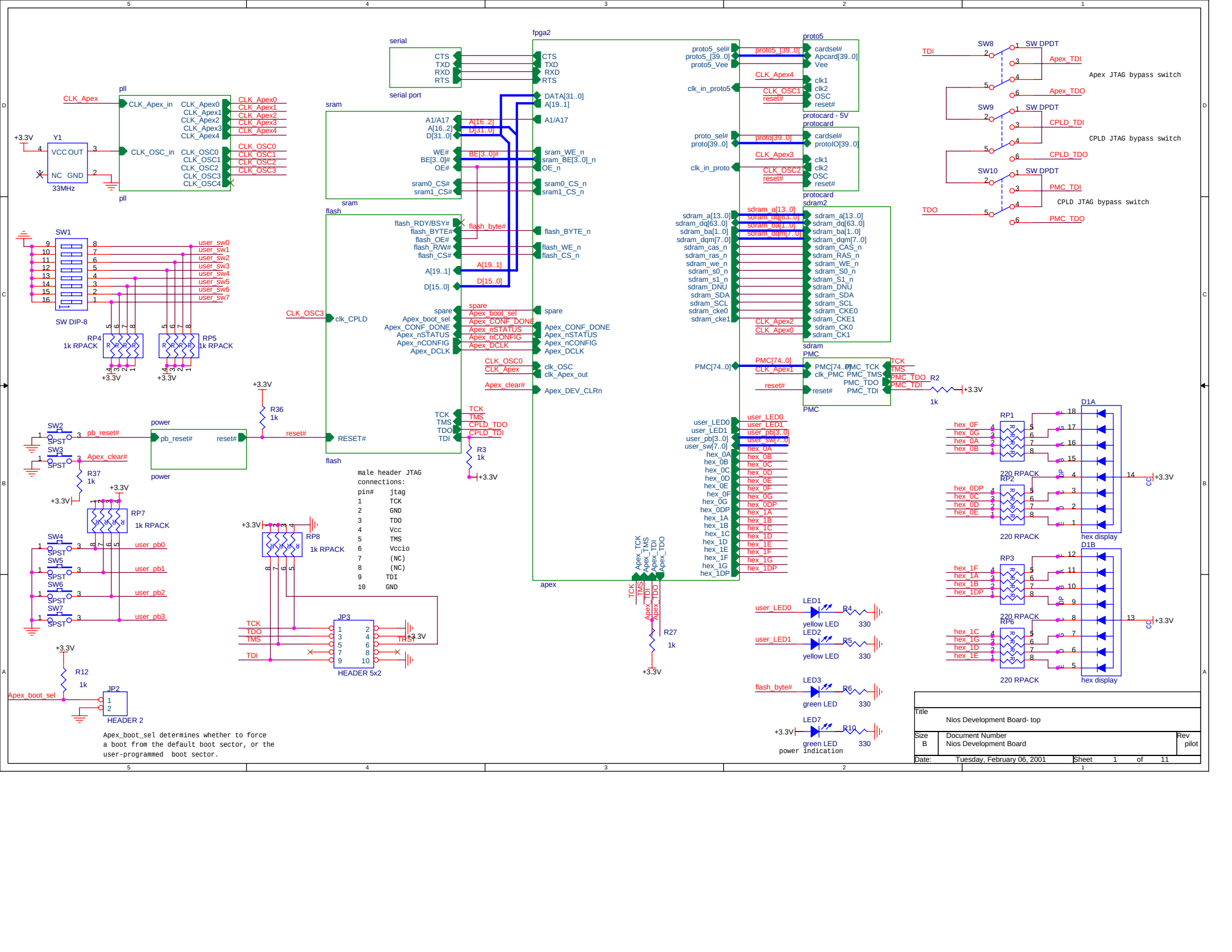
pll
CLK_Apex
CLK_Apex_in
CLK_Apex0
CLK_Apex1
CLK_Apex2
CLK_Apex3
CLK_Apex4
CLK_OSC_in
CLK_OSC0
CLK_OSC1
CLK_OSC2
CLK_OSC3
CLK_OSC4
+3.3V
Y1
VCC OUT
NC GND
33MHz
serial
CTS
TXD
RXD
RTS
serial port
fpga2
sram
A1/A17
A[16..2]
D[31..0]
WE#
BE[3..0]#
OE#
sram0_CS#
sram1_CS#
sram_WE_n
sram_BE[3..0]_n
OE_n
sram0_CS_n
sram1_CS_n
DATA[31..0]
A[19..1]
flash
flash_RDY/BSY#
flash_BYTE#
flash_OE#
flash_R/W#
flash_CS#
flash_byte#
flash_BYTE_n
flash_WE_n
flash_CS_n
D[15..0]
spare
Apex_boot_sel
Apex_CONF_DONE
Apex_nSTATUS
Apex_nCONFIG
Apex_DCLK
clk_CPLD
clk_OSC
clk_Apex_out
Apex_clear#
Apex_DEV_CLRn
TCK
TMS
CPLD_TDO
CPLD_TDI
TDI
RESET#
R3
1k
SW1
SW DIP-8
user_sw0
user_sw1
user_sw2
user_sw3
user_sw4
user_sw5
user_sw6
user_sw7
RP4
1k RPACK
RP5
1k RPACK
power
pb_reset#
reset#
R36
SW2
SW3
SPST
R37
RP7
SW4
SW5
SW6
SW7
user_pb0
user_pb1
user_pb2
user_pb3
RP8
JP3
HEADER 5x2
male header JTAG
connections:
pin# jtag
1 TCK
2 GND
3 TDO
4 Vcc
5 TMS
6 Vccio
7 (NC)
8 (NC)
9 TDI
10 GND
R12
Apex_boot_sel
JP2
HEADER 2
Apex_boot_sel determines whether to force
a boot from the default boot sector, or the
user-programmed boot sector.
apex
Apex_TCK
Apex_TMS
Apex_TDI
Apex_TDO
R27
proto5
proto5_sel#
proto5_[39..0]
proto5_Vee
cardsel#
Apcard[39..0]
Vee
CLK_Apex4
clk_in_proto5
CLK_OSC1
reset#
clk1
clk2
OSC
protocard - 5V
protocard
proto_sel#
proto[39..0]
protoIO[39..0]
CLK_Apex3
clk_in_proto
CLK_OSC2
protocard
sdram2
sdram_a[13..0]
sdram_dq[63..0]
sdram_ba[1..0]
sdram_dqm[7..0]
sdram_cas_n
sdram_ras_n
sdram_we_n
sdram_s0_n
sdram_s1_n
sdram_DNU
sdram_SDA
sdram_SCL
sdram_cke0
sdram_cke1
sdram_CAS_n
sdram_RAS_n
sdram_WE_n
sdram_S0_n
sdram_S1_n
sdram_CKE0
sdram_CKE1
sdram_CK0
sdram_CK1
CLK_Apex2
CLK_Apex0
sdram
PMC
PMC[74..0]
CLK_Apex1
PMC_TCK
clk_PMC
PMC_TMS
PMC_TDO
PMC_TDI
R2
user_LED0
user_LED1
user_pb[3..0]
user_sw[7..0]
hex_0A
hex_0B
hex_0C
hex_0D
hex_0E
hex_0F
hex_0G
hex_0DP
hex_1A
hex_1B
hex_1C
hex_1D
hex_1E
hex_1F
hex_1G
hex_1DP
LED1
LED2
LED3
LED7
yellow LED
green LED
R4
R5
R6
R10
330
flash_byte#
power indication
SW8
SW9
SW10
SW DPDT
TDI
TDO
Apex_TDI
Apex_TDO
CPLD_TDI
CPLD_TDO
PMC_TDI
PMC_TDO
Apex JTAG bypass switch
CPLD JTAG bypass switch
CPLD JTAG bypass switch
RP1
RP2
RP3
RP6
220 RPACK
D1A
D1B
hex display
hex_0F
hex_0G
hex_0A
hex_0B
hex_0DP
hex_0C
hex_0D
hex_0E
hex_1F
hex_1A
hex_1B
hex_1DP
hex_1C
hex_1G
hex_1D
hex_1E
Title
Nios Development Board- top
Size
B
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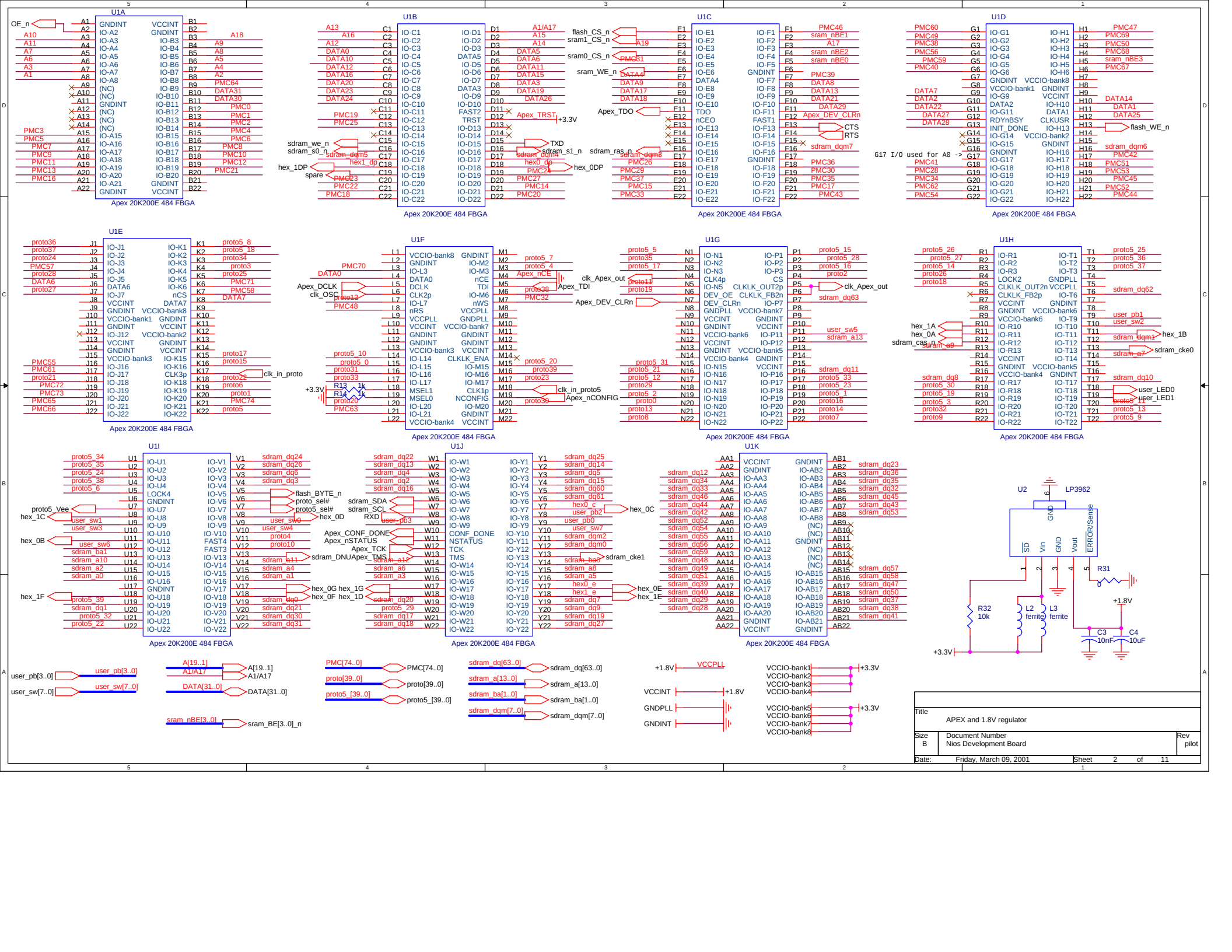
U1A
U1B
U1C
U1D
U1E
U1F
U1G
U1H
U1I
U1J
U1K
Apex 20K200E 484 FBGA
U2
LP3962
R31
R32
10k
L2
ferrite
L3
ferrite
C3
10nF
C4
10uF
+1.8V
+3.3V
Title
APEX and 1.8V regulator
Size
B
Document Number
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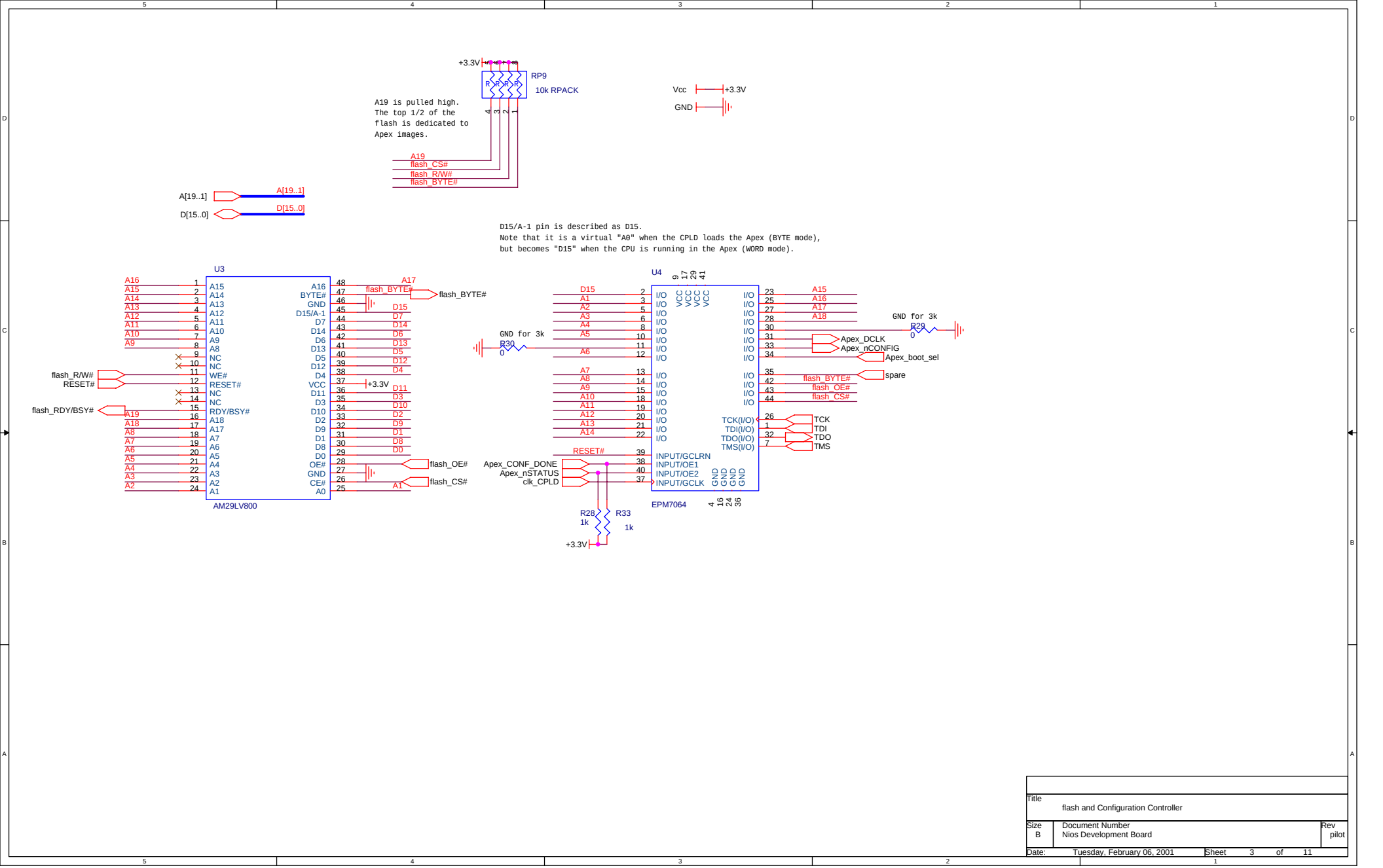

Title	flash and Configuration Controller	
Size B	Document Number Nios Development Board	Rev pilot
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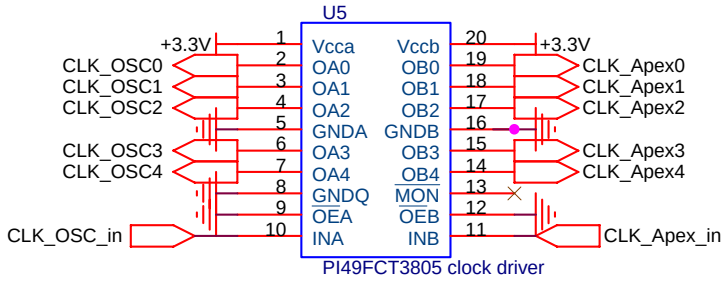
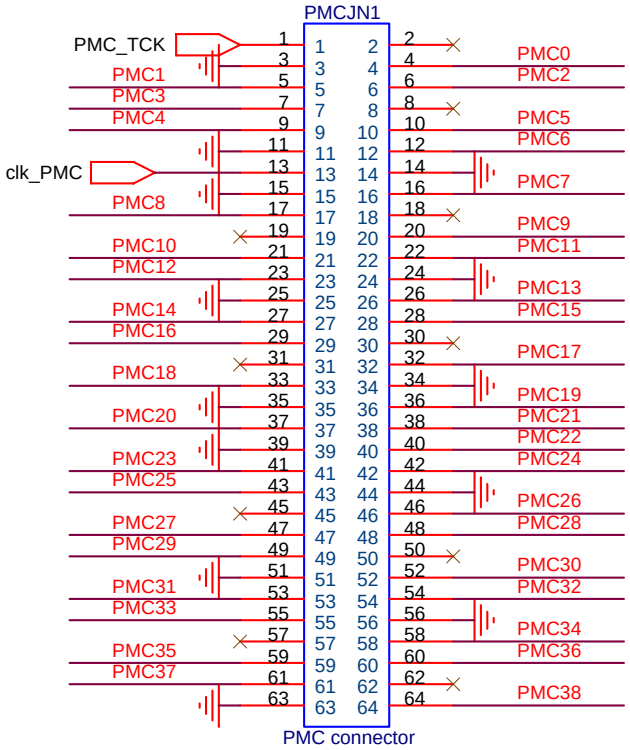
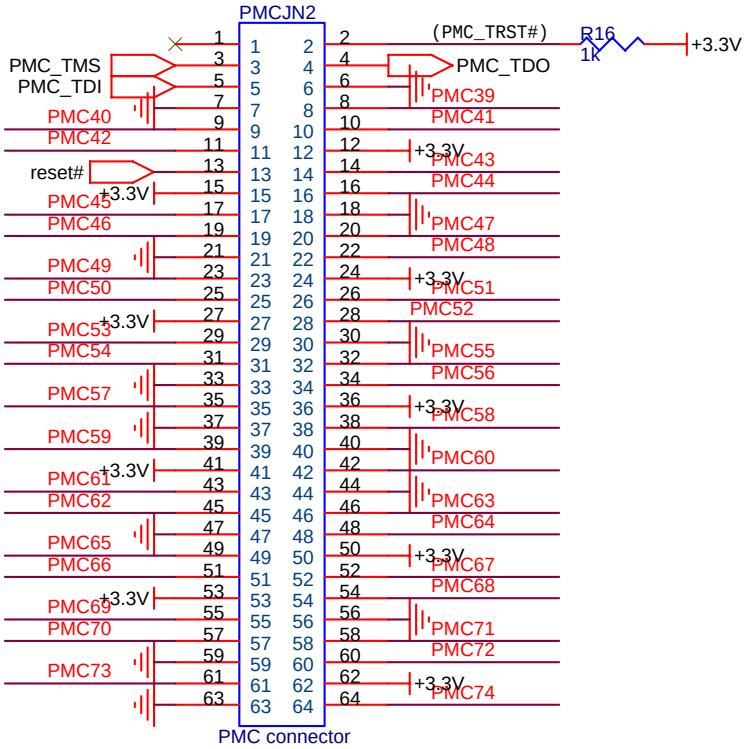
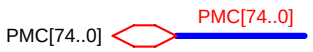


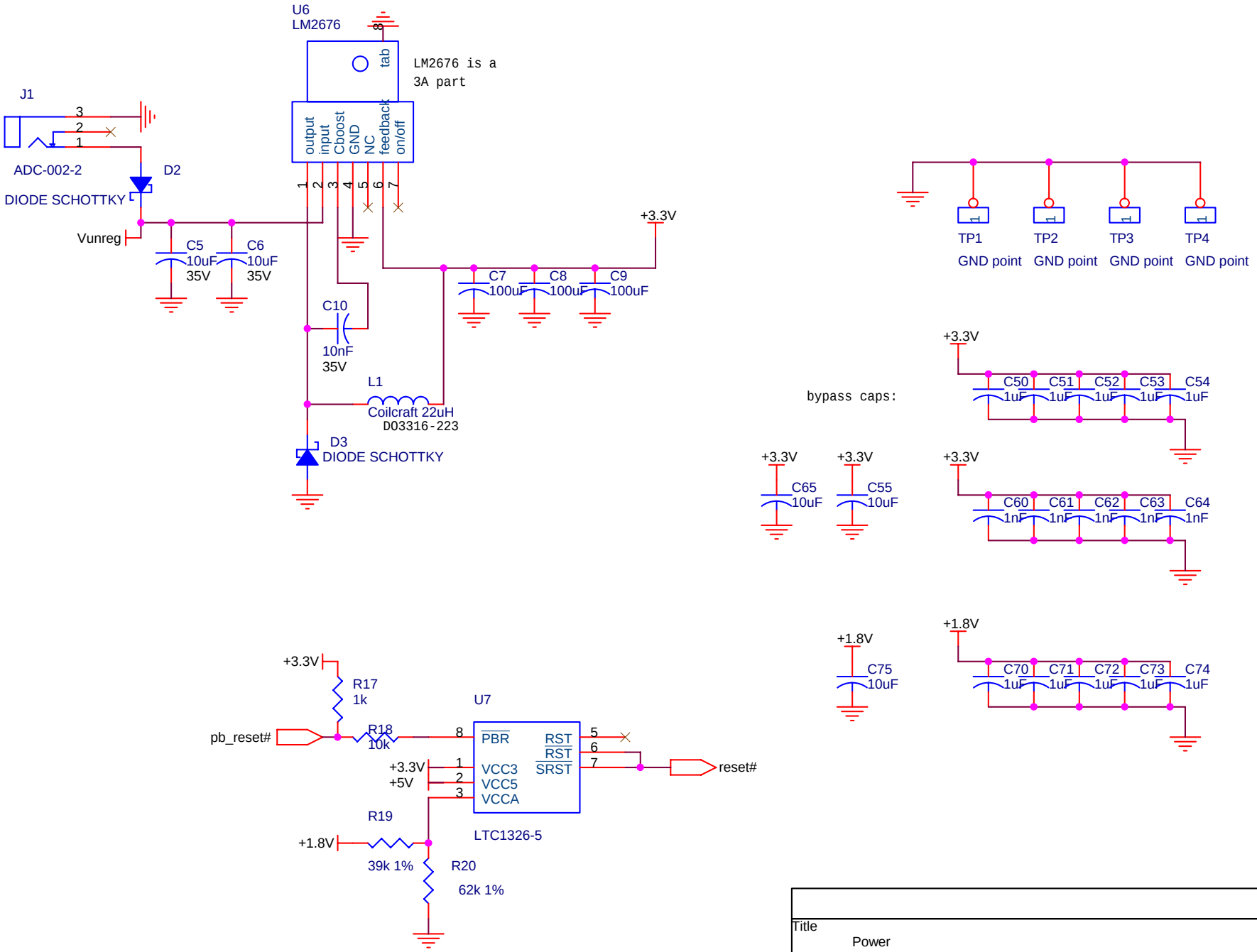
Title	Clock Distribution PLL	
Size A	Document Number Nios Development Board	Rev pilot
Date: Tuesday, February 06, 2001	Sheet 4 of 11	







Title	PMC connectors	
Size A	Document Number Nios Development Board	Rev pilot
Date: Tuesday, February 06, 2001	Sheet 5 of 11	



Title	Power	
Size A	Document Number Nios Development Board	Rev pilot
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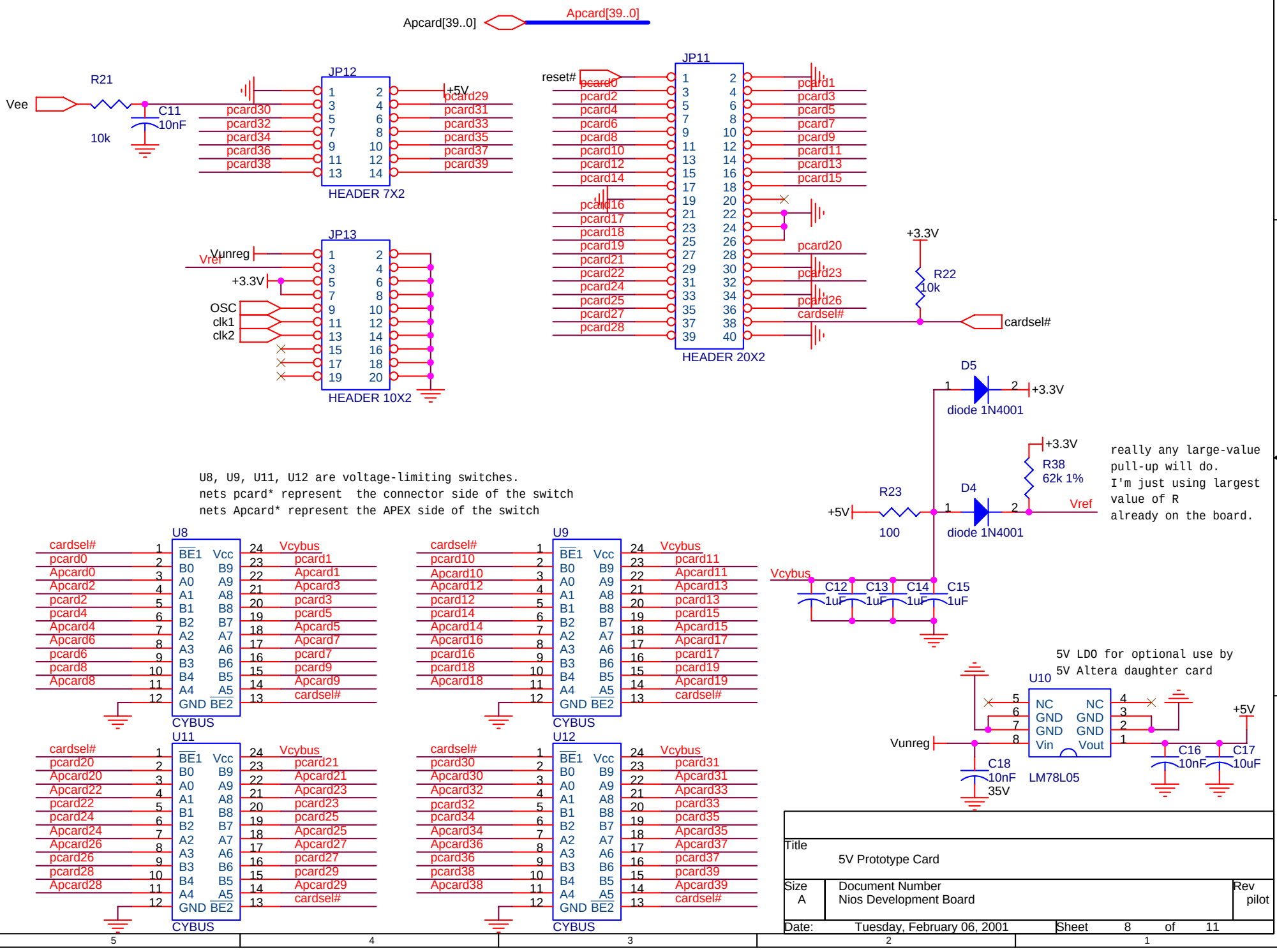
protoIO[39..0] protoIO[39..0]

JP9
HEADER 7X2
protoIO30 protoIO29
protoIO32 protoIO31
protoIO34 protoIO33
protoIO36 protoIO35
protoIO38 protoIO37
protoIO39

JP10
HEADER 10X2
Vunreg
+3.3V
OSC
clk1
clk2

JP8
HEADER 20X2
reset#
protoIO0 protoIO1
protoIO2 protoIO3
protoIO4 protoIO5
protoIO6 protoIO7
protoIO8 protoIO9
protoIO10 protoIO11
protoIO12 protoIO13
protoIO14 protoIO15
protoIO16
protoIO17
protoIO18
protoIO19 protoIO20
protoIO21 protoIO23
protoIO22
protoIO24
protoIO25 protoIO26
protoIO27 cardsel#
protoIO28
+3.3V
R34
10k
cardsel#

Title	3.3V Prototype Card	
Size A	Document Number Nios Development Board	Rev pilot
Date: Tuesday, February 06, 2001	Sheet 7 of 11	


Apcard[39..0]
Apcard[39..0]
JP12
HEADER 7X2
JP11
HEADER 20X2
JP13
HEADER 10X2
R21
10k
C11
10nF
Vee
R22
10k
cardsel#
D5
diode 1N4001
+3.3V
R38
62k 1%
Vref
R23
100
D4
diode 1N4001
+5V
C12
C13
C14
C15
1uF
Vcybus
really any large-value
pull-up will do.
I'm just using largest
value of R
already on the board.
U8, U9, U11, U12 are voltage-limiting switches.
nets pcard* represent the connector side of the switch
nets Apcard* represent the APEX side of the switch
U8
U9
U11
U12
CYBUS
5V LDO for optional use by
5V Altera daughter card
U10
LM78L05
C16
10nF
C17
10uF
C18
10nF
35V
Vunreg
Title
5V Prototype Card
Size
A
Document Number
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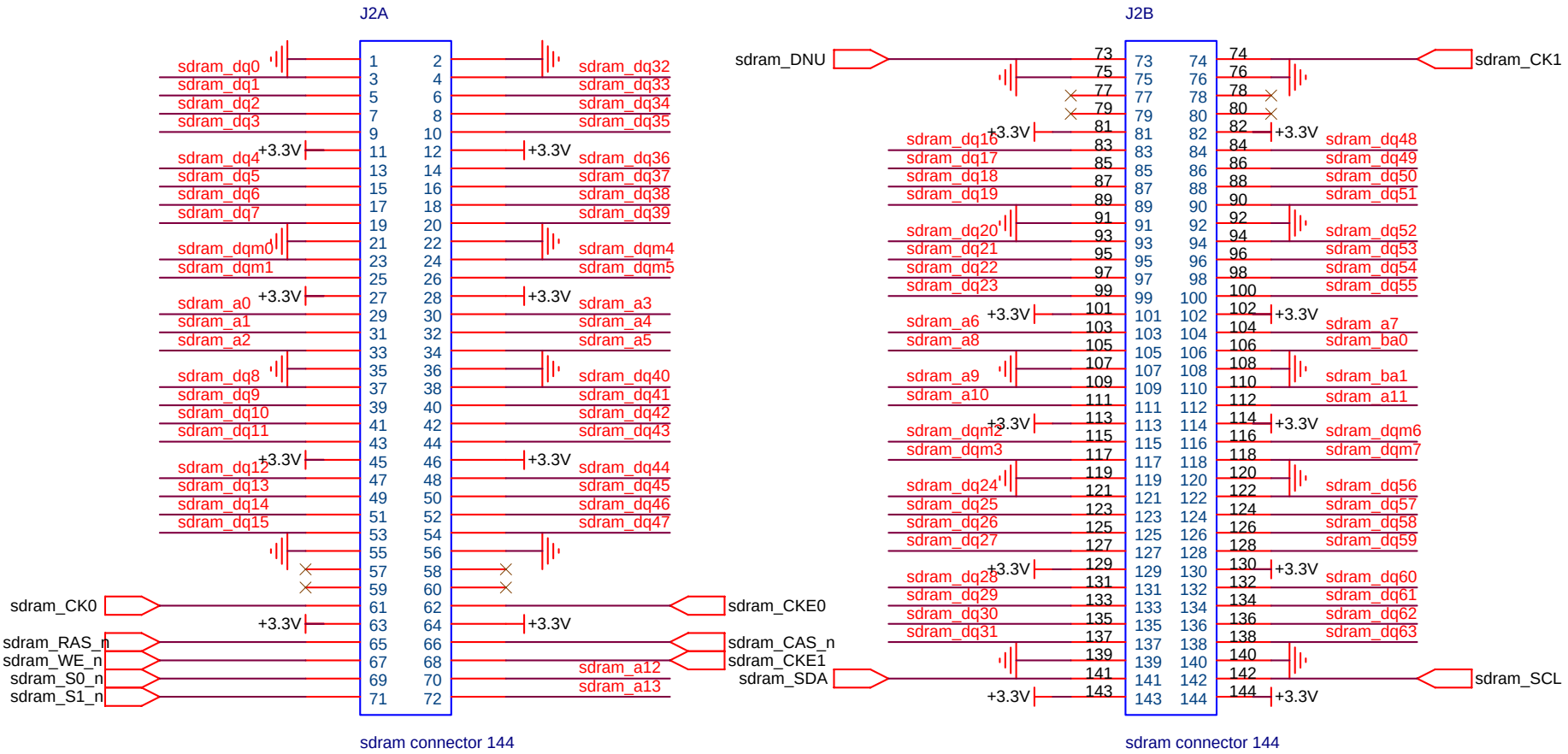
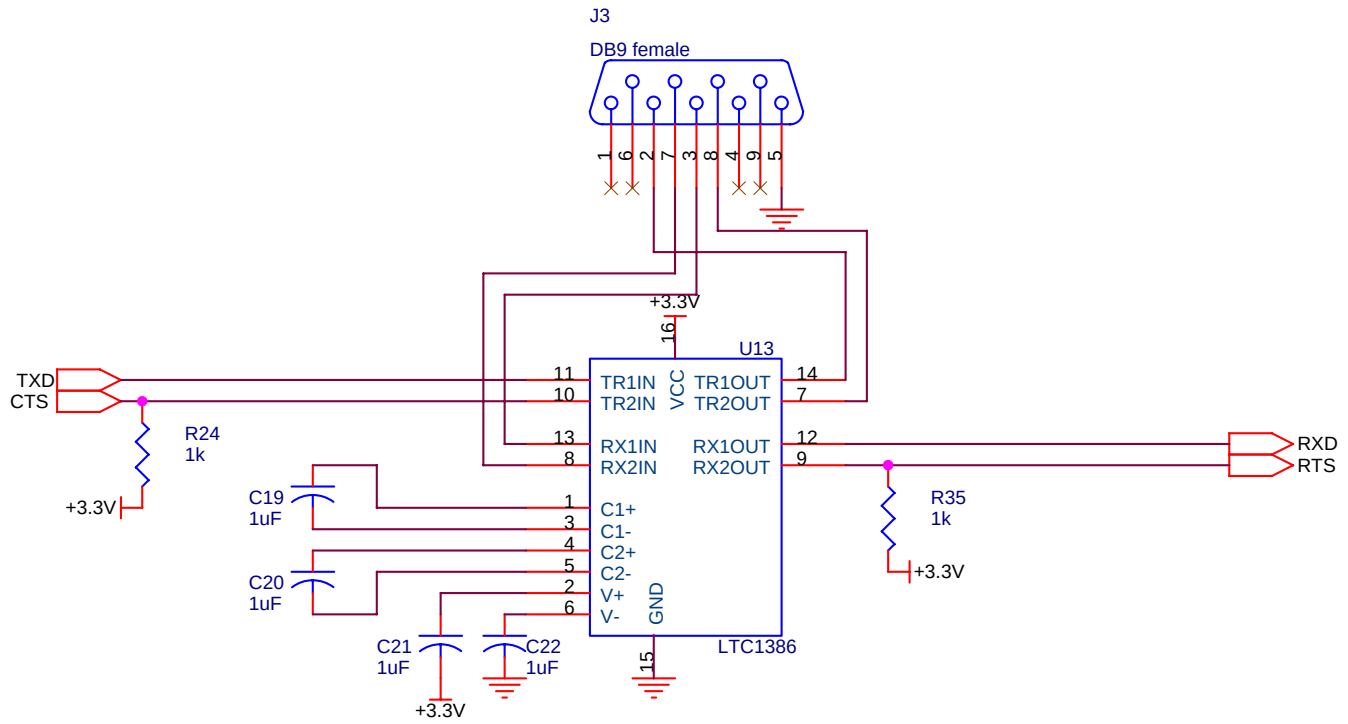
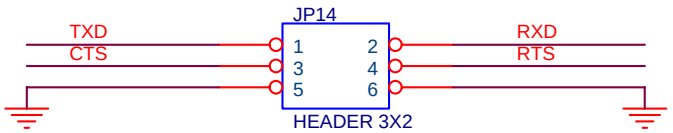
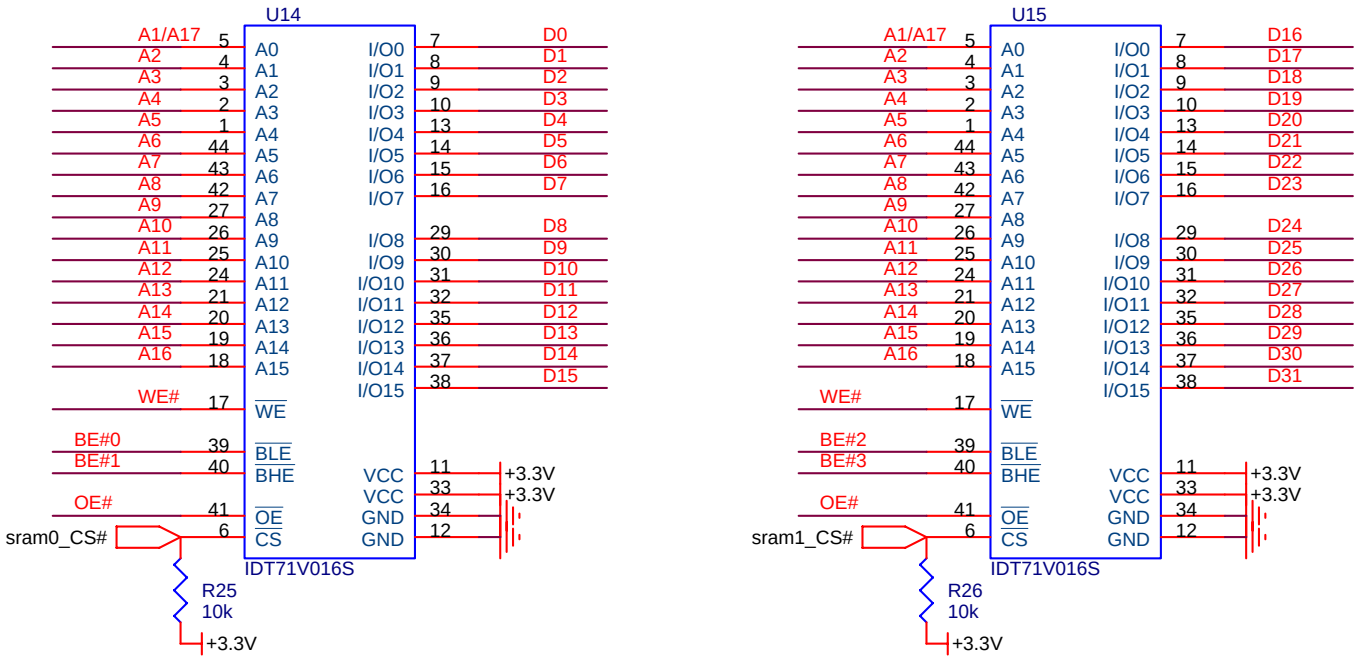


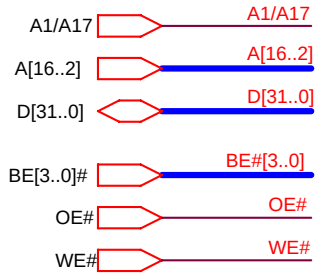
Title	SODIMM SDRAM connector	
Size A	Document Number Nios Development Board	Rev pilot
Date: Tuesday, February 06, 2001	Sheet 9 of 11	





Title: Serial Port		
Size: A	Document Number: Nios Development Board	Rev: pilot
Date: Tuesday, February 06, 2001	Sheet 10 of 11	





Title: SRAM		
Size: A	Document Number: Nios Development Board	Rev: pilot
Date: Tuesday, February 06, 2001	Sheet 11 of 11	