

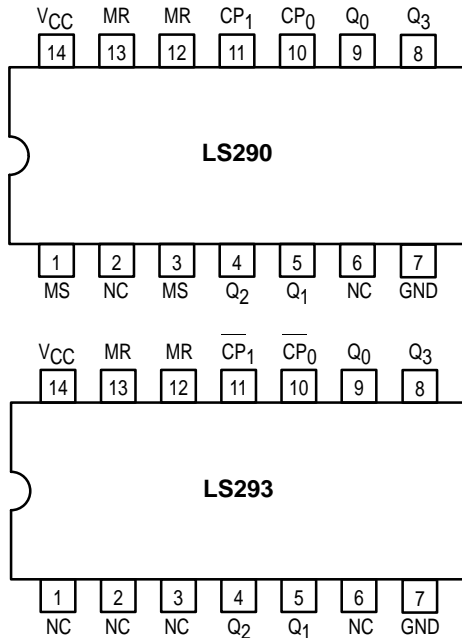


DECADE COUNTER; 4-BIT BINARY COUNTER

The SN54/74LS290 and SN54/74LS293 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS290) or divide-by-eight (LS293) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to CP) to form BCD, Bi-quinary, or Modulo-16 counters. Both of the counters have a 2-input gated Master Reset (Clear), and the LS290 also has a 2-input gated Master Set (Preset 9).

- Corner Power Pin Versions of the LS90 and LS93
- Low Power Consumption . . . Typically 45 mW
- High Count Rates . . . Typically 42 MHz
- Choice of Counting Modes . . . BCD, Bi-Quinary, Binary
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

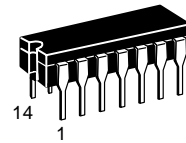
| | |
|--|--|
| CP ₀ | Clock (Active LOW going edge) Input to +2 Section. |
| CP ₁ | Clock (Active LOW going edge) Input to +5 Section (LS290). |
| CP ₁ | Clock (Active LOW going edge) Input to +8 Section (LS293). |
| MR1, MR2 | Master Reset (Clear) Inputs |
| MS1, MS2 | Master Set (Preset-9, LS290) Inputs |
| Q ₀ | Output from +2 Section (Notes b & c) |
| Q ₁ , Q ₂ , Q ₃ | Outputs from +5 & +8 Sections (Note b) |

NOTES:

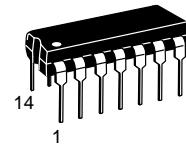
- a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
 c) The Q₀ Outputs are guaranteed to drive the full fan-out plus the CP₁ Input of the device.

SN54/74LS290 SN54/74LS293

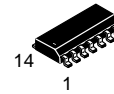
DECADE COUNTER; 4-BIT BINARY COUNTER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

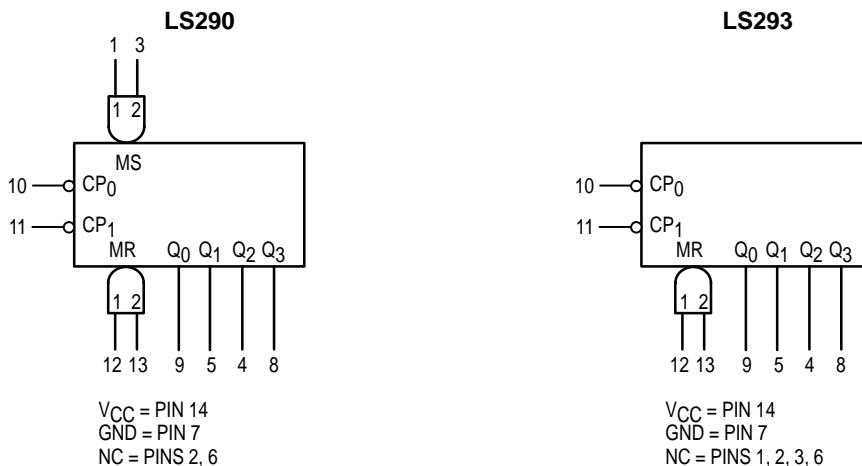
| | |
|------------|---------|
| SN54LSXXXJ | Ceramic |
| SN74LSXXXN | Plastic |
| SN74LSXXXD | SOIC |

LOADING (Note a)

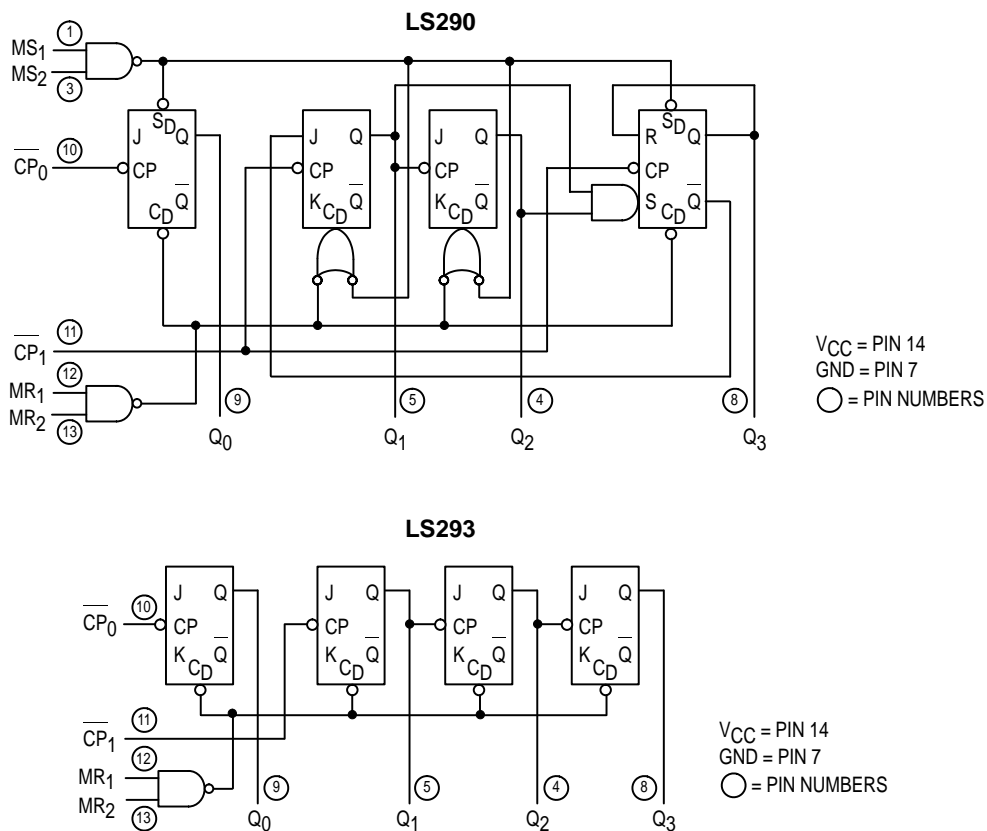
| HIGH | LOW |
|-----------|--------------|
| 0.05 U.L. | 1.5 U.L. |
| 0.05 U.L. | 2.0 U.L. |
| 0.05 U.L. | 1.0 U.L. |
| 0.5 U.L. | 0.25 U.L. |
| 0.5 U.L. | 0.25 U.L. |
| 10 U.L. | 5 (2.5) U.L. |
| 10 U.L. | 5 (2.5) U.L. |

SN54/74LS290 • SN54/74LS293

LOGIC SYMBOL



LOGIC DIAGRAMS



SN54/74LS290 • SN54/74LS293

FUNCTIONAL DESCRIPTION

The LS290 and LS293 are 4-bit ripple type Decade, and 4-Bit Binary counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS290) or divide-by-eight (LS293) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q₀ output of each device is designed and specified to drive the rated fan-out plus the CP₁ input of the device.

A gated AND asynchronous Master Reset (MR₁ · MR₂) is provided on both counters which overrides the clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set (MS₁ · MS₂) is provided on the LS290 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

LS290

A. BCD Decade (8421) Counter — the CP₁ input must be

externally connected to the Q₀ output. The CP₀ input receives the incoming count and a BCD count sequence is produced.

- B. Symmetrical Bi-quinary Divide-By-Ten Counter — The Q₃ output must be externally connected to the CP₀ input. The input count is then applied to the CP₁ input and a divide-by-ten square wave is obtained at output Q₀.
- C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function (CP₀ as the input and Q₀ as the output). The CP₁ input is used to obtain binary divide-by-five operation at the Q₃ output.

LS293

- A. 4-Bit Ripple Counter — The output Q₀ must be externally connected to input CP₁. The input count pulses are applied to input CP₀. Simultaneous division of 2, 4, 8, and 16 are performed at the Q₀, Q₁, Q₂, and Q₃ outputs as shown in the truth table.
- B. 3-Bit Ripple Counter — The input count pulses are applied to input CP₁. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q₁, Q₂, and Q₃ outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

LS290 MODE SELECTION

| RESET/SET INPUTS | | | | OUTPUTS | | | |
|------------------|-----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|
| MR ₁ | MR ₂ | MS ₁ | MS ₂ | Q ₀ | Q ₁ | Q ₂ | Q ₃ |
| H | H | L | X | L | L | L | L |
| H | H | X | L | L | L | L | L |
| X | X | H | H | H | L | L | H |
| L | X | L | X | | | Count | |
| X | L | X | L | | | Count | |
| L | X | X | L | | | Count | |
| X | L | L | X | | | Count | |

LS293 MODE SELECTION

| RESET INPUTS | | OUTPUTS | | | |
|-----------------|-----------------|----------------|----------------|----------------|----------------|
| MR ₁ | MR ₂ | Q ₀ | Q ₁ | Q ₂ | Q ₃ |
| H | H | L | L | L | L |
| L | H | | | Count | |
| H | L | | | Count | |
| L | L | | | Count | |

LS290
BCD COUNT SEQUENCE

| COUNT | OUTPUT | | | |
|-------|----------------|----------------|----------------|----------------|
| | Q ₀ | Q ₁ | Q ₂ | Q ₃ |
| 0 | L | L | L | L |
| 1 | H | L | L | L |
| 2 | L | H | L | L |
| 3 | H | H | L | L |
| 4 | L | L | H | L |
| 5 | H | L | H | L |
| 6 | L | H | H | L |
| 7 | H | H | H | L |
| 8 | L | L | L | H |
| 9 | H | L | L | H |

NOTE: Output Q₀ is connected to Input CP₁ for BCD count.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TRUTH TABLE

| COUNT | OUTPUT | | | |
|-------|----------------|----------------|----------------|----------------|
| | Q ₀ | Q ₁ | Q ₂ | Q ₃ |
| 0 | L | L | L | L |
| 1 | H | L | L | L |
| 2 | L | H | L | L |
| 3 | H | H | L | L |
| 4 | L | L | H | L |
| 5 | H | L | H | L |
| 6 | L | H | H | L |
| 7 | H | H | H | L |
| 8 | L | L | L | H |
| 9 | H | L | L | H |
| 10 | L | H | L | H |
| 11 | H | H | L | H |
| 12 | L | L | H | H |
| 13 | H | L | H | H |
| 14 | L | H | H | H |
| 15 | H | H | H | H |

Note: Output Q₀ connected to input CP₁.

SN54/74LS290 • SN54/74LS293

GUARANTEED OPERATING RANGES

| Symbol | Parameter | | Min | Typ | Max | Unit |
|-----------------|-------------------------------------|----------|-------------|------------|-------------|------|
| V _{CC} | Supply Voltage | 54 74 | 4.5 4.75 | 5.0 5.0 | 5.5 5.25 | V |
| T _A | Operating Ambient Temperature Range | 54 74 | -55 0 | 25 25 | 125 70 | °C |
| I _{OH} | Output Current — High | 54, 74 | | | -0.4 | mA |
| I _{OL} | Output Current — Low | 54 74 | | | 4.0 8.0 | mA |

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol | Parameter | Limits | | | Unit | Test Conditions | |
|-----------------|--|--------|-------|------|------|--|---|
| | | Min | Typ | Max | | | |
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs | |
| V _{IL} | Input LOW Voltage | 54 | | 0.7 | V | Guaranteed Input LOW Voltage for All Inputs | |
| | | 74 | | 0.8 | | | |
| V _{IK} | Input Clamp Diode Voltage | | -0.65 | -1.5 | V | V _{CC} = MIN, I _{IN} = -18 mA | |
| V _{OH} | Output HIGH Voltage | 54 | 2.5 | 3.5 | V | V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table | |
| | | 74 | 2.7 | 3.5 | V | | |
| V _{OL} | Output LOW Voltage | 54, 74 | | 0.25 | 0.4 | V | I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table |
| | | 74 | | 0.35 | 0.5 | V | |
| I _{IH} | Input HIGH Current | | | 20 | μA | V _{CC} = MAX, V _{IN} = 2.7 V | |
| | | | | 0.1 | mA | V _{CC} = MAX, V _{IN} = 7.0 V | |
| I _{IL} | Input LOW Current MS, MR CP ₀ CP ₁ (LS290) CP ₁ (LS293) | | | -0.4 | mA | V _{CC} = MAX, V _{IN} = 0.4 V | |
| | | | | -2.4 | | | |
| | | | | -3.2 | | | |
| | | | | -1.6 | | | |
| I _{OS} | Short Circuit Current (Note 1) | -20 | | -100 | mA | V _{CC} = MAX | |
| I _{CC} | Power Supply Current | | | 15 | mA | V _{CC} = MAX | |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS290 • SN54/74LS293

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, C_L = 15 pF)

| Symbol | Parameter | Limits | | | | | | Unit |
|--------------------------------------|--|--------|----------|----------|-------|----------|----------|------|
| | | LS290 | | | LS293 | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| f _{MAX} | CP ₀ Input Clock Frequency | 32 | | | 32 | | | MHz |
| f _{MAX} | CP ₁ Input Clock Frequency | 16 | | | 16 | | | MHz |
| t _{PLH} t _{PHL} | Propagation Delay, CP ₀ Input to Q ₀ Output | | 10 12 | 16 18 | | 10 12 | 16 18 | ns |
| t _{PLH} t _{PHL} | $\overline{\text{CP}}_0$ Input to Q ₃ Output | | 32 34 | 48 50 | | 46 46 | 70 70 | ns |
| t _{PLH} t _{PHL} | $\overline{\text{CP}}_1$ Input to Q ₁ Output | | 10 14 | 16 21 | | 10 14 | 16 21 | ns |
| t _{PLH} t _{PHL} | $\overline{\text{CP}}_1$ Input to Q ₂ Output | | 21 23 | 32 35 | | 21 23 | 32 35 | ns |
| t _{PLH} t _{PHL} | $\overline{\text{CP}}_1$ Input to Q ₃ Output | | 21 23 | 32 35 | | 34 34 | 51 51 | ns |
| t _{PHL} | MS Input to Q ₀ and Q ₃ Outputs | | 20 | 30 | | | | ns |
| t _{PHL} | MS Input to Q ₁ and Q ₂ Outputs | | 26 | 40 | | | | ns |
| t _{PHL} | MR Input to Any Output | | 26 | 40 | | 26 | 40 | ns |

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

| Symbol | Parameter | Limits | | | | Unit |
|------------------|-----------------------------|--------|-----|-------|-----|------|
| | | LS290 | | LS293 | | |
| | | Min | Max | Min | Max | |
| t _W | CP ₀ Pulse Width | 15 | | 15 | | ns |
| t _W | CP ₁ Pulse Width | 30 | | 30 | | ns |
| t _W | MS Pulse Width | 15 | | | | ns |
| t _W | MR Pulse Width | 15 | | 15 | | ns |
| t _{rec} | Recovery Time MR to CP | 25 | | 25 | | ns |

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

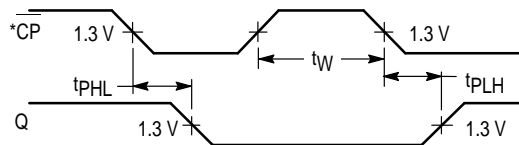


Figure 1

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

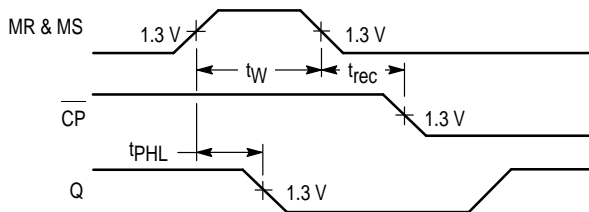


Figure 2

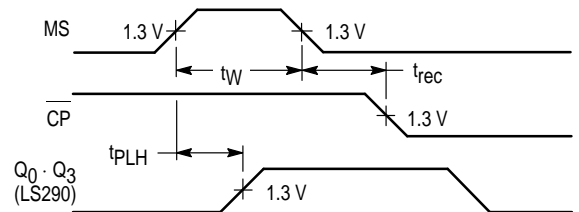


Figure 3