## 8-Input Multiplexer

## Features

- Buffered Inputs
- Typical Propagation Delay
- 6 ns at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$
- Exceeds 2kV ESD Protection MIL-STD-883, Method 3015
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption
- Balanced Propagation Delays
- AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30\% of the Supply
- $\pm 24 m A$ Output Drive Current
- Fanout to 15 FAST ${ }^{\text {TM }}$ ICs
- Drives $50 \Omega$ Transmission Lines


## Description

The CD74AC151 and 'ACT151 are 8-input digital multiplexers that utilize Advanced CMOS Logic technology. They have three binary control inputs (S0, S1, and S2) and an active-LOW Enable ( $\overline{\mathrm{E}}$ ) input. The three binary inputs select 1 of 8 channels. The output is both inverting $(\overline{\mathrm{Y}})$ and noninverting (Y).

## Ordering Information

| PART <br> NUMBER | TEMP. <br> RANGE $\left({ }^{\circ} \mathrm{C}\right)$ | PACKAGE |
| :--- | :---: | :--- |
| CD74AC151E | 0 to $70^{\circ} \mathrm{C},-40$ to 85, <br> -55 to 125 | 16 Ld PDIP |
| CD74AC151M96 | 0 to $70^{\circ} \mathrm{C},-40$ to 85, <br> -55 to 125 | 16 Ld SOIC |
| CD54ACT151F3A | -55 to 125 | 16 Ld CERDIP |
| CD74ACT151E | 0 to $70^{\circ} \mathrm{C},-40$ to 85, <br> -55 to 125 | 16 Ld PDIP |
| CD74ACT151M96 | 0 to $70^{\circ} \mathrm{C},-40$ to 85, <br> -55 to 125 | 16 Ld SOIC |

## NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

## Pinout



## Functional Diagram



TRUTH TABLE

| INPUTS |  |  |  |  |  |  |  |  |  |  |  | OUTPUTS |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\overline{\mathrm{E}}$ | $\mathrm{S}_{2}$ | $\mathrm{S}_{1}$ | $\mathrm{S}_{0}$ | $\mathrm{I}_{0}$ | $\mathrm{I}_{1}$ | $\mathrm{I}_{2}$ | $\mathrm{I}_{3}$ | $\mathrm{I}_{4}$ | $\mathrm{I}_{5}$ | $\mathrm{I}_{6}$ | $\mathrm{I}_{7}$ | $\overline{\mathrm{Y}}$ | Y |
| H | X | X | X | X | X | X | X | X | X | X | X | H | L |
| L | L | L | L | L | X | X | X | X | X | X | X | H | L |
| L | L | L | L | H | X | X | X | X | X | X | X | L | H |
| L | L | L | H | X | L | X | X | X | X | X | X | H | L |
| L | L | L | H | X | H | X | X | X | X | X | X | L | H |
| L | L | H | L | X | X | L | X | X | X | X | X | H | L |
| L | L | H | L | X | X | H | X | X | X | X | X | L | H |
| L | L | H | H | X | X | X | L | X | X | X | X | H | L |
| L | L | H | H | X | X | X | H | X | X | X | X | L | H |
| L | H | L | L | X | X | X | X | L | X | X | X | H | L |
| L | H | L | L | X | X | X | X | H | X | X | X | L | H |
| L | H | L | H | X | X | X | X | X | L | X | X | H | L |
| L | H | L | H | X | X | X | X | X | H | X | X | L | H |
| L | H | H | L | X | X | X | X | X | X | L | X | H | L |
| L | H | H | L | X | X | X | X | X | X | H | X | L | H |
| L | H | H | H | X | X | X | X | X | X | X | L | H | L |
| L | H | H | H | X | X | X | X | X | X | X | H | L | H |

$\mathrm{H}=\mathrm{HIGH}$ voltage level, $\mathrm{L}=\mathrm{LOW}$ voltage level, $\mathrm{X}=$ Don't Care


Thermal Information
Thermal Resistance (Typical, Note 5) $\quad \theta_{\mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
PDIP Package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 90
SOIC Package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 160
Maximum Junction Temperature (Plastic Package) . . . . . . . . . . $150^{\circ} \mathrm{C}$
Maximum Storage Temperature Range . . . . . . . . . $65^{\circ} \mathrm{C}$ to $150^{\circ} \mathrm{C}$
Maximum Lead Temperature (Soldering 10s) . . . . . . . . . . . . . $300^{\circ} \mathrm{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## NOTES:

3. For up to 4 outputs per device, add $\pm 25 \mathrm{~mA}$ for each additional output.
4. Unless otherwise specified, all voltages are referenced to ground.
5. $\theta_{\mathrm{JA}}$ is measured with the component mounted on an evaluation PC board in free air.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS |  | $\begin{aligned} & V_{C C} \\ & \text { (V) } \end{aligned}$ | $25^{\circ} \mathrm{C}$ |  | $\begin{gathered} -40^{\circ} \mathrm{C} \text { TO } \\ 85^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{gathered} -55^{\circ} \mathrm{C} \text { TO } \\ 125^{\circ} \mathrm{C} \end{gathered}$ |  | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{V}_{1}(\mathrm{~V})$ | 10 (mA) |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| AC TYPES |  |  |  |  |  |  |  |  |  |  |  |
| High Level Input Voltage | $\mathrm{V}_{\mathrm{IH}}$ | - | - | 1.5 | 1.2 | - | 1.2 | - | 1.2 | - | V |
|  |  |  |  | 3 | 2.1 | - | 2.1 | - | 2.1 | - | V |
|  |  |  |  | 5.5 | 3.85 | - | 3.85 | - | 3.85 | - | V |
| Low Level Input Voltage | $\mathrm{V}_{\mathrm{IL}}$ | - | - | 1.5 | - | 0.3 | - | 0.3 | - | 0.3 | V |
|  |  |  |  | 3 | - | 0.9 | - | 0.9 | - | 0.9 | V |
|  |  |  |  | 5.5 | - | 1.65 | - | 1.65 | - | 1.65 | V |
| High Level Output Voltage | $\mathrm{V}_{\mathrm{OH}}$ | $\mathrm{V}_{\mathrm{IH}}$ or $\mathrm{V}_{\mathrm{IL}}$ | -0.05 | 1.5 | 1.4 | - | 1.4 | - | 1.4 | - | V |
|  |  |  | -0.05 | 3 | 2.9 | - | 2.9 | - | 2.9 | - | V |
|  |  |  | -0.05 | 4.5 | 4.4 | - | 4.4 | - | 4.4 | - | V |
|  |  |  | -4 | 3 | 2.58 | - | 2.48 | - | 2.4 | - | V |
|  |  |  | -24 | 4.5 | 3.94 | - | 3.8 | - | 3.7 | - | V |
|  |  |  | $\begin{gathered} -75 \\ (\text { Note } 6,7) \end{gathered}$ | 5.5 | - | - | 3.85 | - | - | - | V |
|  |  |  | $\begin{gathered} -50 \\ (\text { Note 6, 7) } \end{gathered}$ | 5.5 | - | - | - | - | 3.85 | - | V |

## DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS |  | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}} \\ & \text { (V) } \end{aligned}$ | $25^{\circ} \mathrm{C}$ |  | $\begin{gathered} -40^{\circ} \mathrm{C} \text { TO } \\ 85^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{gathered} -55^{\circ} \mathrm{C} \text { TO } \\ 125^{\circ} \mathrm{C} \end{gathered}$ |  | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{V}_{1}(\mathrm{~V})$ | $\mathrm{I}_{0}(\mathrm{~mA})$ |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| Low Level Output Voltage | $\mathrm{V}_{\mathrm{OL}}$ | $\mathrm{V}_{\mathrm{IH}}$ or $\mathrm{V}_{\mathrm{IL}}$ | 0.05 | 1.5 | - | 0.1 | - | 0.1 | - | 0.1 | V |
|  |  |  | 0.05 | 3 | - | 0.1 | - | 0.1 | - | 0.1 | V |
|  |  |  | 0.05 | 4.5 | - | 0.1 | - | 0.1 | - | 0.1 | V |
|  |  |  | 12 | 3 | - | 0.36 | - | 0.44 | - | 0.5 | V |
|  |  |  | 24 | 4.5 | - | 0.36 | - | 0.44 | - | 0.5 | V |
|  |  |  | 75 <br> (Note 6, 7) | 5.5 | - | - | - | 1.65 | - | - | V |
|  |  |  | $\begin{array}{c\|} \hline 50 \\ (\text { Note } 6,7) \end{array}$ | 5.5 | - | - | - | - | - | 1.65 | V |
| Input Leakage Current | I | $\mathrm{V}_{\mathrm{CC}}$ or GND | - | 5.5 | - | $\pm 0.1$ | - | $\pm 1$ | - | $\pm 1$ | $\mu \mathrm{A}$ |
| Quiescent Supply Current MSI | ICC | $\begin{gathered} \mathrm{V}_{\mathrm{CC}} \text { or } \\ \mathrm{GND} \end{gathered}$ | 0 | 5.5 | - | 8 | - | 80 | - | 160 | $\mu \mathrm{A}$ |


| High Level Input Voltage | $\mathrm{V}_{\mathrm{IH}}$ | - | - | $\begin{gathered} 4.5 \text { to } \\ 5.5 \end{gathered}$ | 2 | - | 2 | - | 2 | - | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Low Level Input Voltage | $\mathrm{V}_{\text {IL }}$ | - | - | $\begin{gathered} \hline 4.5 \text { to } \\ 5.5 \end{gathered}$ | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage | $\mathrm{V}_{\mathrm{OH}}$ | $\mathrm{V}_{\mathrm{IH}}$ or $\mathrm{V}_{\mathrm{IL}}$ | -0.05 | 4.5 | 4.4 | - | 4.4 | - | 4.4 | - | V |
|  |  |  | -24 | 4.5 | 3.94 | - | 3.8 | - | 3.7 | - | V |
|  |  |  | $\begin{gathered} -75 \\ (\text { Note 6, 7) } \end{gathered}$ | 5.5 | - | - | 3.85 | - | - | - | V |
|  |  |  | $\begin{gathered} -50 \\ (\text { Note 6, 7) } \end{gathered}$ | 5.5 | - | - | - | - | 3.85 | - | V |
| Low Level Output Voltage | $\mathrm{V}_{\mathrm{OL}}$ | $\mathrm{V}_{\mathrm{IH}}$ or $\mathrm{V}_{\mathrm{IL}}$ | 0.05 | 4.5 | - | 0.1 | - | 0.1 | - | 0.1 | V |
|  |  |  | 24 | 4.5 | - | 0.36 | - | 0.44 | - | 0.5 | V |
|  |  |  | $\begin{gathered} 75 \\ (\text { Note 6, 7) } \end{gathered}$ | 5.5 | - | - | - | 1.65 | - | - | V |
|  |  |  | $\begin{gathered} 50 \\ \text { (Note 6, 7) } \end{gathered}$ | 5.5 | - | - | - | - | - | 1.65 | V |
| Input Leakage Current | 1 | $\begin{aligned} & \hline \mathrm{V}_{\mathrm{CC}} \text { or } \\ & \mathrm{GND} \end{aligned}$ | - | 5.5 | - | $\pm 0.1$ | - | $\pm 1$ | - | $\pm 1$ | $\mu \mathrm{A}$ |
| Quiescent Supply Current MSI | ${ }^{\text {I CC }}$ | $\begin{aligned} & \hline \mathrm{V}_{\mathrm{CC}} \text { or } \\ & \mathrm{GND} \end{aligned}$ | 0 | 5.5 | - | 8 | - | 80 | - | 160 | $\mu \mathrm{A}$ |
| Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load | $\Delta^{\text {I CC }}$ | $\begin{aligned} & \hline \mathrm{V}_{\mathrm{CC}} \\ & -2.1 \end{aligned}$ | - | $\begin{gathered} \hline 4.5 \text { to } \\ 5.5 \end{gathered}$ | - | 2.4 | - | 2.8 | - | 3 | mA |

NOTES:
6. Test one output at a time for a 1 -second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
7. Test verifies a minimum $50 \Omega$ transmission-line-drive capability at $85^{\circ} \mathrm{C}, 75 \Omega$ at $125^{\circ} \mathrm{C}$.

## ACT Input Load Table

| INPUT | UNIT LOAD |
| :---: | :---: |
| I (All) | 1 |
| $\overline{\mathrm{E}}$ | 1 |
| S | 1 |

NOTE: Unit load is $\Delta_{\text {CC }}$ limit specified in DC Electrical Specifications Table, e.g., 2.4 mA max at $25^{\circ} \mathrm{C}$.

Switching Specifications Input $\mathrm{t}_{\mathrm{r}}, \mathrm{t}_{\mathrm{f}}=3 \mathrm{~ns}, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ (Worst Case)

| PARAMETER | SYMBOL | $\mathrm{V}_{\mathrm{cc}}(\mathrm{V})$ | $-40^{\circ} \mathrm{C} \mathrm{TO} 85{ }^{\circ} \mathrm{C}$ |  |  | ${ }^{-55}{ }^{\circ} \mathrm{C}$ TO $125^{\circ} \mathrm{C}$ |  |  | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| AC TYPES |  |  |  |  |  |  |  |  |  |
| Propagation Delay, Any Data to Y | $\mathrm{t}_{\text {PLH }}$, $\mathrm{t}_{\text {PHL }}$ | 1.5 | - | - | 152 | - | - | 169 | ns |
|  |  | $\begin{gathered} 3.3 \\ \text { (Note 9) } \end{gathered}$ | 4.9 | - | 17.1 | 4.7 | - | 18.9 | ns |
|  |  | $\begin{gathered} \hline 5 \\ \text { (Note 10) } \end{gathered}$ | 3.5 | - | 12.3 | 3.4 | - | 13.5 | ns |
| Propagation Delay, Any Data to $\bar{Y}$ | $\mathrm{t}_{\text {PLH, }}$, tPHL | 1.5 | - | - | 169 | - | - | 186 | ns |
|  |  | 3.3 | 5.4 | - | 19 | 5.2 | - | 20.9 | ns |
|  |  | 5 | 3.8 | - | 13.5 | 3.7 | - | 14.9 | ns |
| Propagation Delay, Any Select to $Y$ | $t_{\text {PLH, }}$, tPHL | 1.5 | - | - | 207 | - | - | 228 | ns |
|  |  | 3.3 | 6.6 | - | 23.2 | 6.4 | - | 25.5 | ns |
|  |  | 5 | 4.7 | - | 16.5 | 4.6 | - | 18.2 | ns |
| Propagation Delay, Any Select to Y | $\mathrm{t}_{\text {PLH }}, \mathrm{t}_{\text {PHL }}$ | 1.5 | - | - | 223 | - | - | 245 | ns |
|  |  | 3.3 | 7.1 | - | 24.9 | 6.9 | - | 27.4 | ns |
|  |  | 5 | 5.1 | - | 17.8 | 4.9 | - | 19.6 | ns |
| Propagation Delay, Any Enable to Y | $\mathrm{t}_{\text {PLH, }}$ t ${ }_{\text {PHL }}$ | 1.5 | - | - | 139 | - | - | 153 | ns |
|  |  | 3.3 | 4.4 | - | 15.5 | 4.3 | - | 17.1 | ns |
|  |  | 5 | 3.1 | - | 11.1 | 3.1 | - | 12.2 | ns |
| Propagation Delay, Any Enable to Y | $\mathrm{t}_{\text {PLH, }}$, ${ }_{\text {PHL }}$ | 1.5 | - | - | 153 | - | - | 169 | ns |
|  |  | 3.3 | 4.9 | - | 17.2 | 4.7 | - | 18.9 | ns |
|  |  | 5 | 3.5 | - | 12.3 | 3.4 | - | 13.5 | ns |
| Input Capacitance | $\mathrm{Cl}_{1}$ | - | - | - | 10 | - | - | 10 | pF |
| Power Dissipation Capacitance | CPD (Note 11) | - | - | 120 | - | - | 120 | - | pF |
| ACT TYPES |  |  |  |  |  |  |  |  |  |
| Propagation Delay, Any Data to Y | ${ }_{\text {tpLH, }}$ tphL | $\begin{gathered} 5 \\ \text { (Note 10) } \end{gathered}$ | 4 | - | 14.1 | 3.9 | - | 15.5 | ns |
| Propagation Delay, Any Data to $\bar{Y}$ | ${ }_{\text {tPLH }}$, tPHL | 5 | 4.4 | - | 15.4 | 4.2 | - | 16.9 | ns |
| Propagation Delay, Any Select to $Y$ | ${ }_{\text {tPLH, }}$ tPHL | 5 | 5.2 | - | 18.4 | 5.1 | - | 20.2 | ns |
| Propagation Delay, Any Select to $\bar{Y}$ | ${ }_{\text {tPLH, }} \mathrm{t}_{\text {PHL }}$ | 5 | 5.6 | - | 19.6 | 5.4 | - | 21.6 | ns |
| Propagation Delay, Any Enable to Y | ${ }_{\text {tPLH, }}$ tPHL | 5 | 3.1 | - | 11 | 3 | - | 12.1 | ns |
| Propagation Delay, Any Enable to $\bar{Y}$ | ${ }_{\text {tPLH, }}$ tPHL | 5 | 3.5 | - | 12.3 | 3.4 | - | 13.5 | ns |
| Input Capacitance | $\mathrm{C}_{1}$ | - | - | - | 10 | - | - | 10 | pF |
| Power Dissipation Capacitance | $\mathrm{C}_{\mathrm{PD}}$ <br> (Note 11) | - | - | 120 | - | - | 120 | - | pF |

## NOTES:

8. Limits tested at $100 \%$.
9. 3.3V Min at 3.6 V , Max at 3 V .
10. 5 V Min at 5.5 V , Max at 4.5 V .
11. $C_{P D}$ is used to determine the dynamic power consumption per device.
$A C: P_{D}=V_{C C}{ }^{2} f_{i}\left(C_{P D}+C_{L}\right)$
$A C T: P_{D}=V_{C C}{ }^{2} f_{i}\left(C_{P D}+C_{L}\right)+V_{C C} \Delta I_{C C}$ where $f_{i}=$ input frequency, $C_{L}=$ output load capacitance, $V_{C C}=$ supply voltage.


FIGURE 1. INPUTS OR SELECT TO OUTPUT PROPAGATION DELAYS


FIGURE 2. ENABLE TO OUTPUT PROPAGATION DELAYS


NOTE: For $A C$ Series Only: When $V_{C C}=1.5 \mathrm{~V}, R_{L}=1 \mathrm{k} \Omega$.

|  | AC | ACT |
| :--- | :---: | :---: |
| Input Level | $\mathrm{V}_{\mathrm{CC}}$ | 3 V |
| Input Switching Voltage, $\mathrm{V}_{\mathrm{S}}$ | $0.5 \mathrm{~V}_{\mathrm{CC}}$ | 1.5 V |
| Output Switching Voltage, $\mathrm{V}_{\mathrm{S}}$ | $0.5 \mathrm{~V}_{\mathrm{CC}}$ | $0.5 \mathrm{~V}_{\mathrm{CC}}$ |

FIGURE 3. PROPAGATION DELAY TIMES

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