

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT190**

**Presettable synchronous BCD  
decade up/down counter**

Product specification  
File under Integrated Circuits, IC06

December 1990

## Presettable synchronous BCD decade up/down counter

### 74HC/HCT190

#### FEATURES

- Synchronous reversible counting
- Asynchronous parallel load
- Count enable control for synchronous expansion
- Single up/down control input
- Output capability: standard
- I<sub>CC</sub> category: MSI

#### GENERAL DESCRIPTION

The 74HC/HCT190 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT190 are asynchronously presettable up/down BCD decade counters. They contain four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel data inputs (D<sub>0</sub> to D<sub>3</sub>) is loaded into the counter and appears on the outputs when the parallel load ( $\overline{PL}$ ) input is LOW. As indicated in the function table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the count enable ( $\overline{CE}$ ) input. When  $\overline{CE}$  is LOW internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The up/down ( $\overline{U/D}$ ) input signal determines the direction of counting as indicated in the function table. The  $\overline{CE}$  input may go LOW when the clock is in either state, however, the LOW-to-HIGH  $\overline{CE}$  transition must occur only when the clock is HIGH. Also, the  $\overline{U/D}$  input should be changed only when either  $\overline{CE}$  or CP is HIGH.

Overflow/underflow indications are provided by two types of outputs, the terminal count (TC) and ripple clock ( $\overline{RC}$ ). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "9" in the count-up-mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until  $\overline{U/D}$  is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the  $\overline{RC}$  output. When TC is HIGH and  $\overline{CE}$  is LOW, the  $\overline{RC}$  output follows the clock pulse (CP). This feature simplifies the design of multistage counters as shown in Figs 5 and 6.

In Fig.5, each  $\overline{RC}$  output is used as the clock input to the next higher stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH on  $\overline{CE}$  inhibits the  $\overline{RC}$  output pulse as indicated in the function table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This can be a disadvantage of this configuration in some applications.

Fig.6 shows a method of causing state changes to occur simultaneously in all stages. The  $\overline{RC}$  outputs propagate the carry/borrow signals in ripple fashion and all clock inputs are driven in parallel. In this configuration the duration of the clock LOW state must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the  $\overline{RC}$  output of any package goes HIGH shortly after its CP input goes HIGH there is no such restriction on the HIGH-state duration of the clock.

In Fig.7, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the  $\overline{CE}$  input for a given stage. An enable must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own  $\overline{CE}$  signal therefore the simple inhibit scheme of Figs 5 and 6 does not apply.

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**QUICK REFERENCE DATA**GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$ 

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay CP to $Q_n$	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	22	24	ns
$f_{max}$	maximum clock frequency		28	30	MHz
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per flip-flop	notes 1 and 2	36	38	pF

**Notes**

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

- For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

**ORDERING INFORMATION**

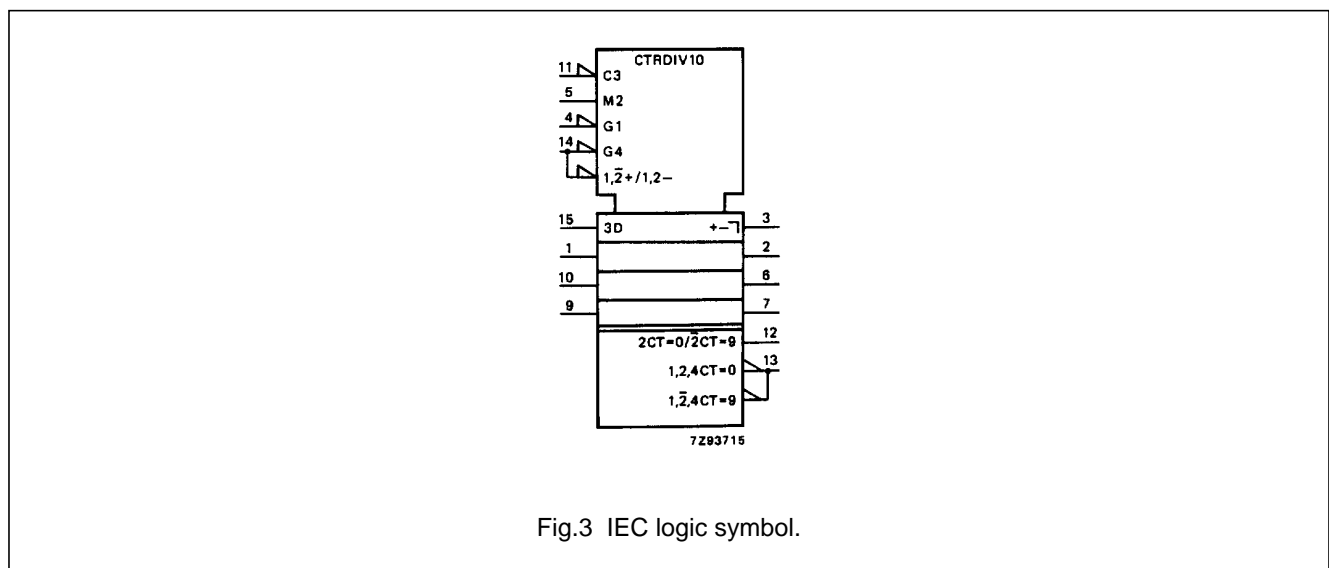
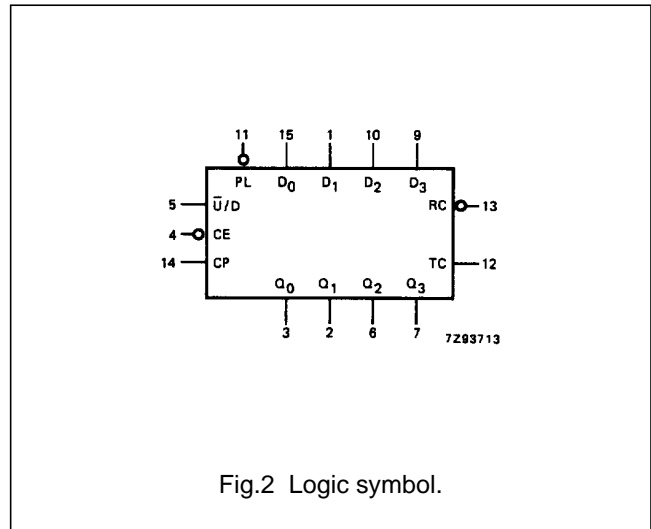
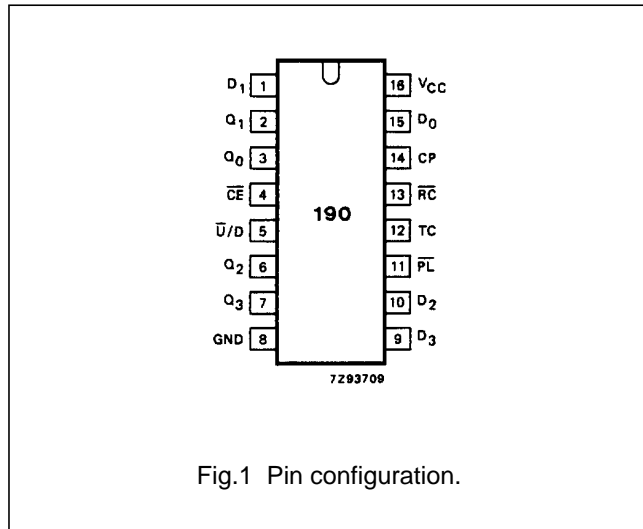
See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q <sub>0</sub> to Q <sub>3</sub>	flip-flop outputs
4	$\overline{CE}$	count enable input (active LOW)
5	$\overline{U/D}$	up/down input
8	GND	ground (0 V)
11	$\overline{PL}$	parallel load input (active LOW)
12	TC	terminal count output
13	$\overline{RC}$	ripple clock output (active LOW)
14	CP	clock input (LOW-to-HIGH, edge-triggered)
15, 1, 10, 9	D <sub>0</sub> to D <sub>3</sub>	data inputs
16	V <sub>CC</sub>	positive supply voltage



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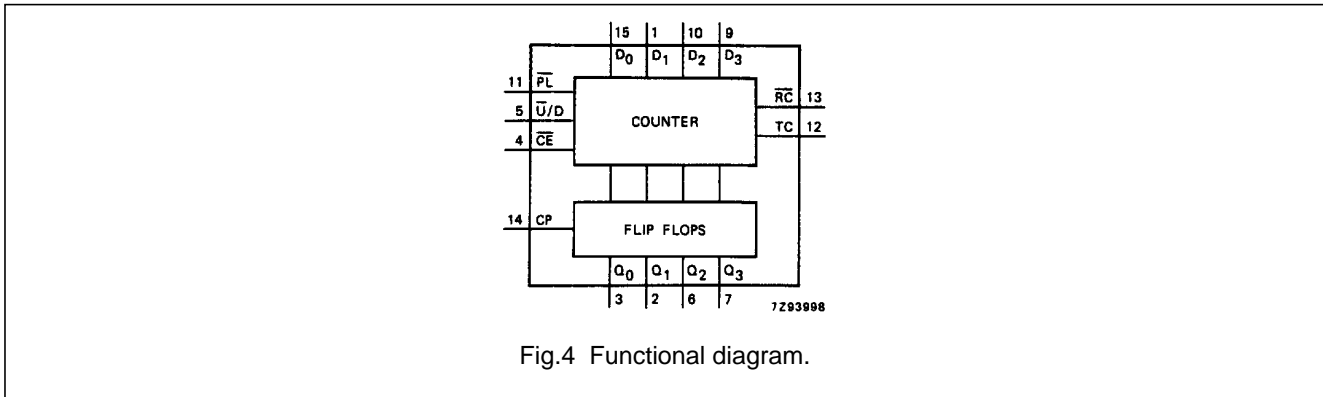


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U/D}$	$\overline{CE}$	CP	$D_n$	$Q_n$
parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
count up	H	L	I	↑	X	count up
count down	H	H	I	↑	X	count down
hold (do nothing)	H	X	H	X	X	no change

TC AND RC FUNCTION TABLE

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U/D}$	$\overline{CE}$	CP	$Q_0$	$Q_1$	$Q_2$	$Q_3$	TC	$\overline{RC}$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L		H	X	X	H		
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L		L	L	L	L		

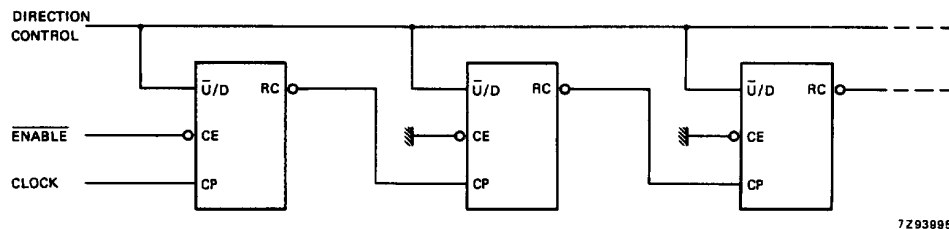
Notes

- H = HIGH voltage level  
 L = LOW voltage level  
 I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 X = don't care  
 ↑ = LOW-to-HIGH CP transition

= one LOW level pulse  
 = TC goes LOW on a LOW-to-HIGH CP transition

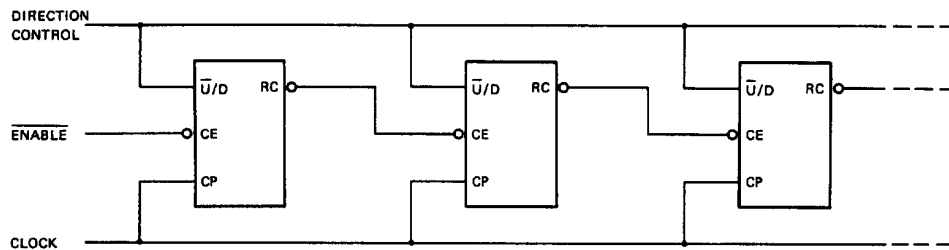
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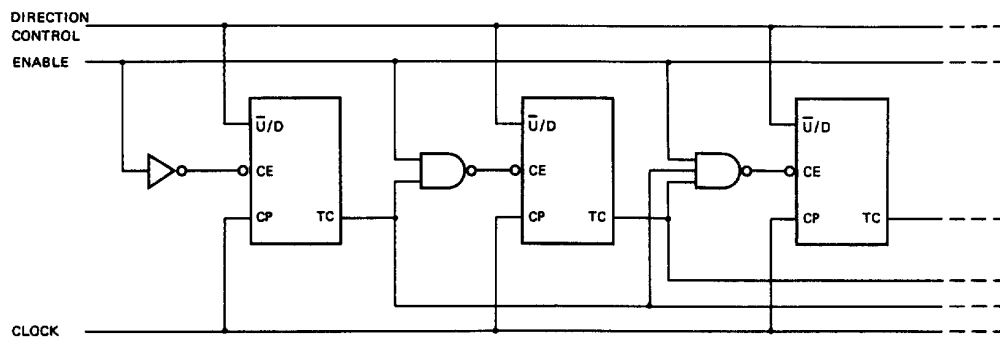
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Fig.5 N-stage ripple counter using ripple clock.



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Fig.6 Synchronous n-stage counter using ripple carry/borrow.



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Fig.7 Synchronous n-stage counter with parallel gated carry/borrow.

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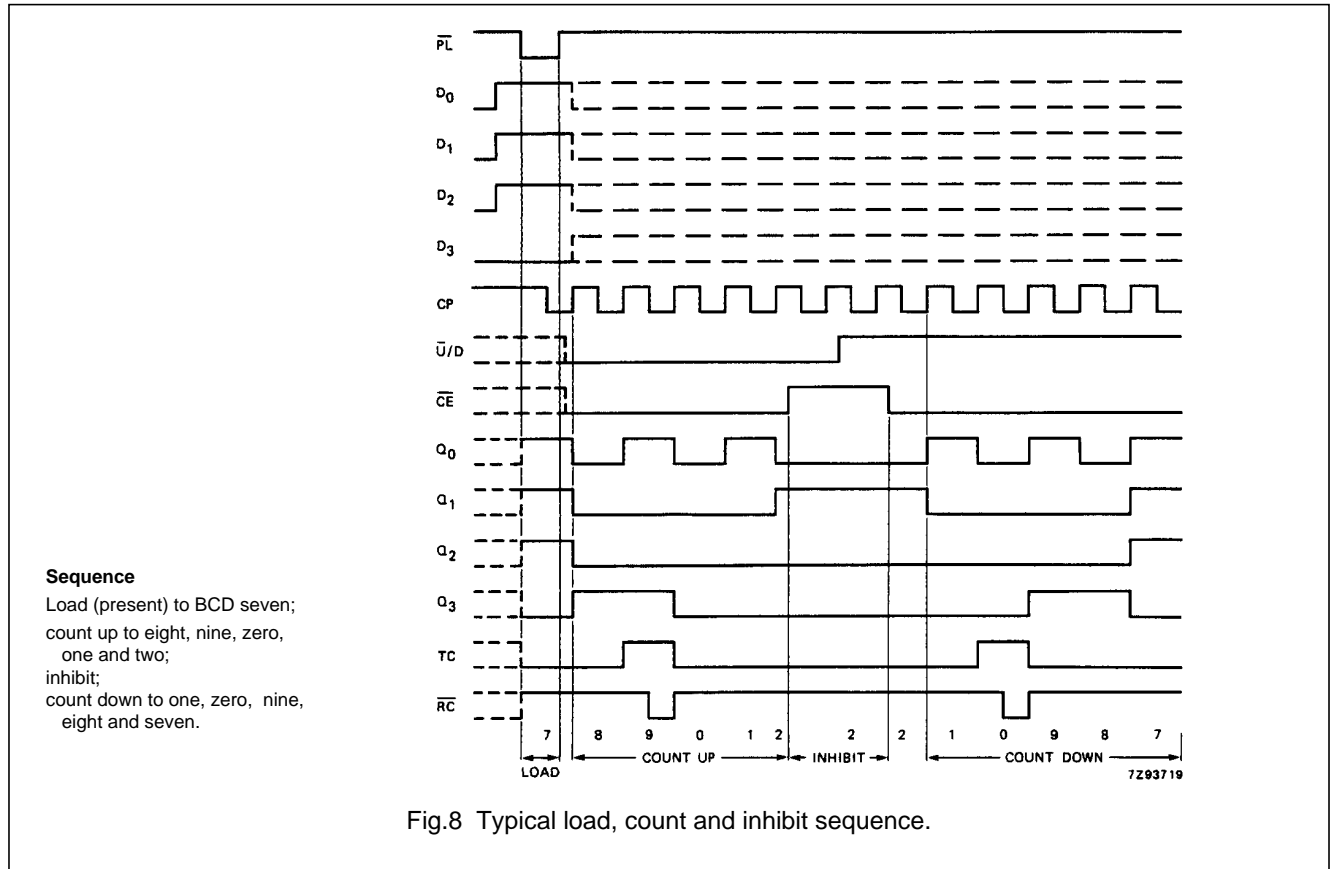


Fig.8 Typical load, count and inhibit sequence.

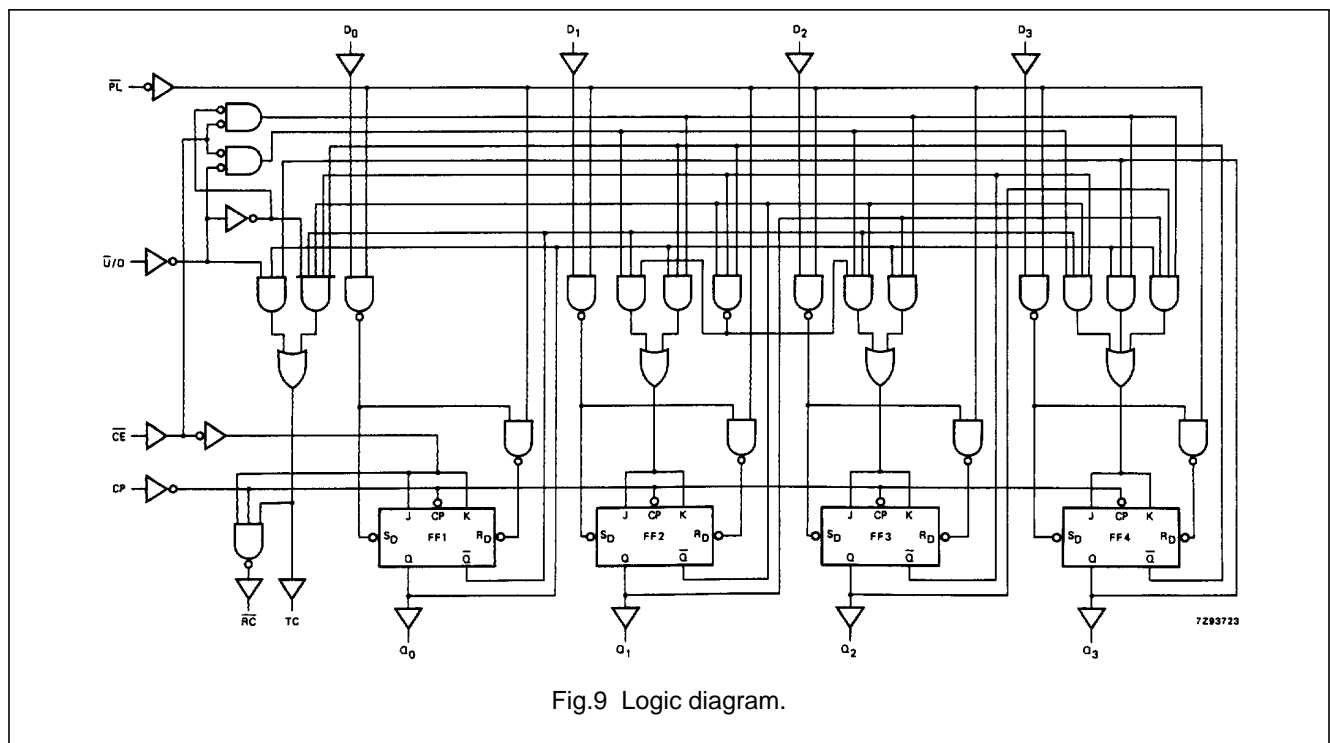


Fig.9 Logic diagram.

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**DC CHARACTERISTICS FOR 74HC**For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 TO +85		-40 TO +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		72 26 21	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig.10
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to TC		83 30 24	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	Fig.10
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to $\overline{RC}$		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.11
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{CE}$ to $\overline{RC}$		33 12 10	130 26 22		165 33 28		195 39 33	ns	2.0 4.5 6.0	Fig.11
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub>		63 23 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig.12
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{PL}$ to Q <sub>n</sub>		63 23 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig.13
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{U/D}$ to TC		44 16 13	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig.14
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{U/D}$ to $\overline{RC}$		50 18 14	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig.14
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.15
t <sub>w</sub>	clock pulse width HIGH or LOW	155 31 26	28 10 8		195 39 33		235 47 40		ns	2.0 4.5 6.0	Fig.10
t <sub>w</sub>	parallel load pulse width LOW	100 20 17	25 9 7		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.15



# Pre-settable synchronous BCD decade up/down counter

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SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 TO +85		-40 TO +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>rem</sub>	removal time $\overline{PL}$ to CP	35 7 6	8 3 2		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig.15
t <sub>su</sub>	set-up time $\overline{U/D}$ to CP	205 41 35	61 22 18		255 51 43		310 62 53		ns	2.0 4.5 6.0	Fig.17
t <sub>su</sub>	set-up time D <sub>n</sub> to $\overline{PL}$	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.16
t <sub>su</sub>	set-up time $\overline{CE}$ to CP	140 28 24	39 14 11		175 35 30		210 42 36		ns	2.0 4.5 6.0	Fig.17
t <sub>h</sub>	hold time $\overline{U/D}$ to CP	0 0 0	-44 -16 -13		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.17
t <sub>h</sub>	hold time D <sub>n</sub> to $\overline{PL}$	0 0 0	-14 -5 -4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.16
t <sub>h</sub>	hold time $\overline{CE}$ to CP	0 0 0	-19 -7 -6		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.17
f <sub>max</sub>	maximum clock pulse frequency	3.0 15 18	8.3 25 30		2.4 12 14		2.0 10 12		MHz	2.0 4.5 6.0	Fig.10

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Presettable synchronous BCD decade  
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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D <sub>n</sub>	0.5
CP	0.65
$\overline{U/D}$	1.15
$\overline{CE}, \overline{PL}$	1.5

# Pre-settable synchronous BCD decade up/down counter

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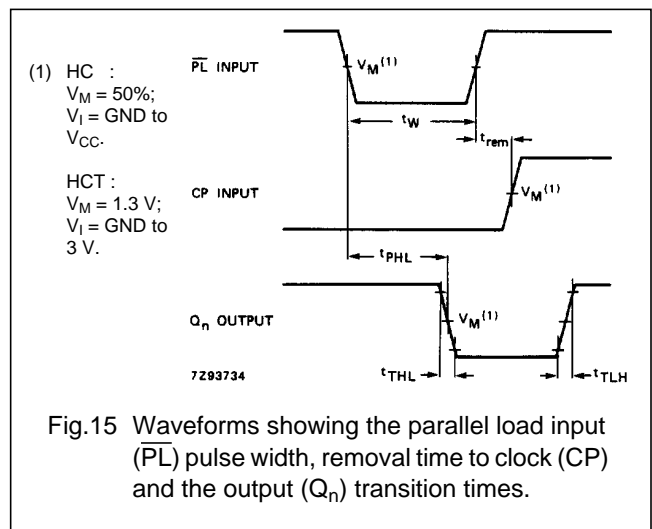
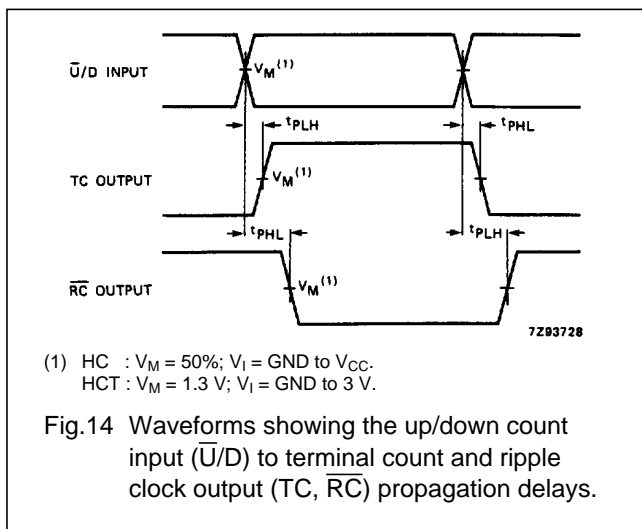
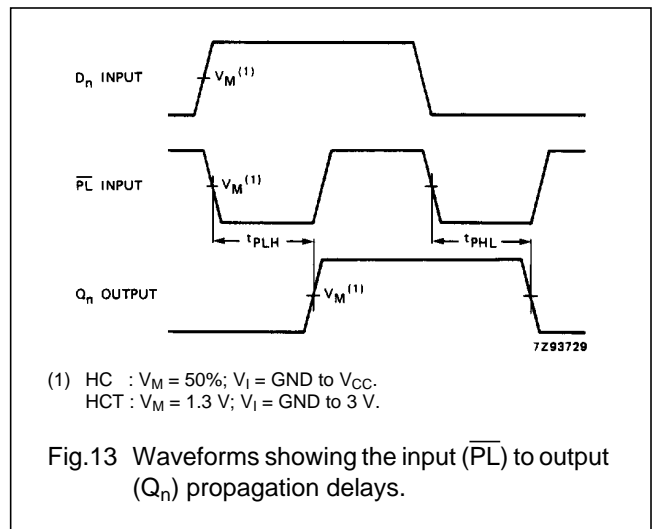
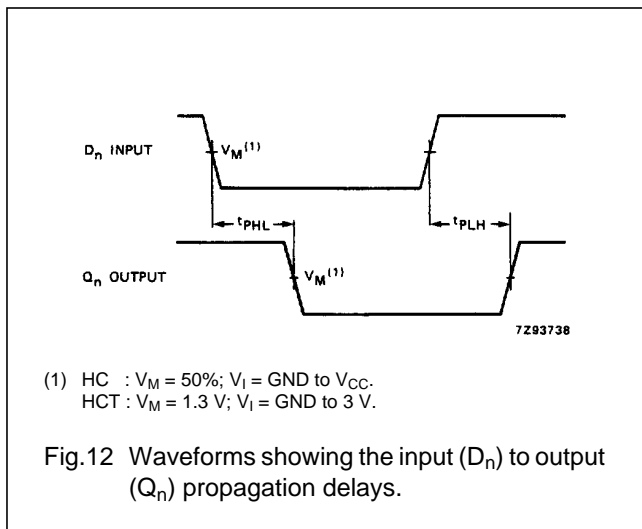
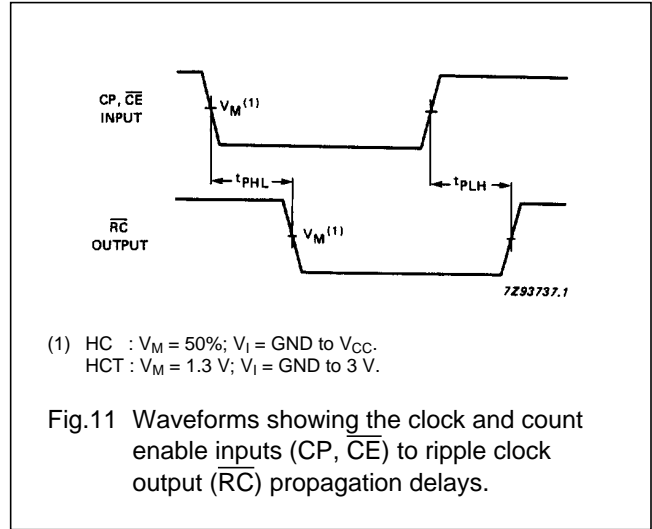
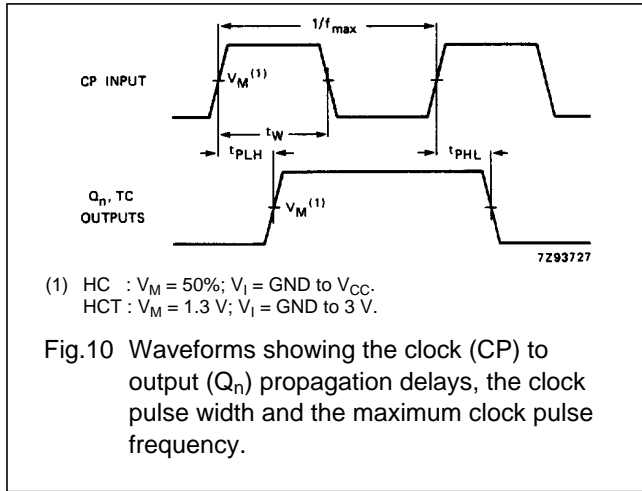
**AC CHARACTERISTICS FOR 74HCT**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)							UNIT	TEST CONDITIONS	
		74HCT								$V_{CC}$ (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
$t_{PHL}/t_{PLH}$	propagation delay CP to $Q_n$		28	48		60		72	ns	4.5	Fig.10
$t_{PHL}/t_{PLH}$	propagation delay CP to TC		34	58		73		87	ns	4.5	Fig.10
$t_{PHL}/t_{PLH}$	propagation delay CP to $\overline{RC}$		20	35		44		53	ns	4.5	Fig.11
$t_{PHL}/t_{PLH}$	propagation delay $\overline{CE}$ to RC		18	33		41		50	ns	4.5	Fig.11
$t_{PHL}/t_{PLH}$	propagation delay $D_n$ to $Q_n$		24	44		55		66	ns	4.5	Fig.12
$t_{PHL}/t_{PLH}$	propagation delay $\overline{PL}$ to $Q_n$		29	49		61		74	ns	4.5	Fig.13
$t_{PHL}/t_{PLH}$	propagation delay $\overline{U/D}$ to TC		24	45		56		68	ns	4.5	Fig.14
$t_{PHL}/t_{PLH}$	propagation delay $\overline{U/D}$ to $\overline{RC}$		26	45		56		68	ns	4.5	Fig.14
$t_{THL}/t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Fig.15
$t_W$	clock pulse width HIGH or LOW	25	10		31		38		ns	4.5	Fig.10
$t_W$	parallel load pulse width LOW	22	12		28		33		ns	4.5	Fig.15
$t_{rem}$	removal time $\overline{PL}$ to CP	7	1		9		11		ns	4.5	Fig.15
$t_{su}$	set-up time $\overline{U/D}$ to CP	42	25		53		63		ns	4.5	Fig.17
$t_{su}$	set-up time $D_n$ to $\overline{PL}$	20	10		25		30		ns	4.5	Fig.16
$t_{su}$	set-up time $\overline{CE}$ to CP	31	18		39		47		ns	4.5	Fig.17
$t_h$	hold time $\overline{U/D}$ to CP	0	-18		0		0		ns	4.5	Fig.17
$t_h$	hold time $D_n$ to $\overline{PL}$	0	-6		0		0		ns	4.5	Fig.16
$t_h$	hold time $\overline{CE}$ to CP	0	-10		0		0		ns	4.5	Fig.17
$f_{max}$	maximum clock pulse frequency	16	27		13		11		MHz	4.5	Fig.10

# Presettable synchronous BCD decade up/down counter

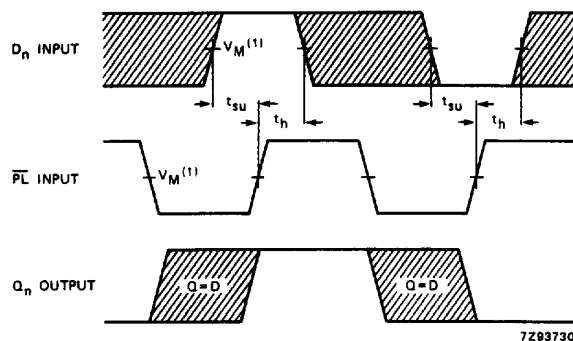
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## AC WAVEFORMS



Pre-settable synchronous BCD decade  
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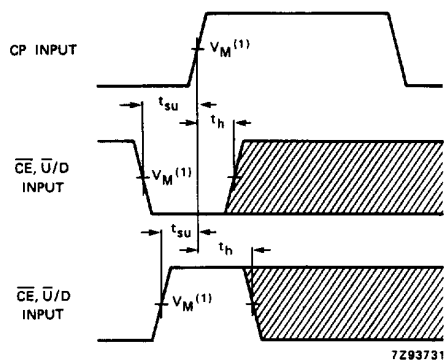
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The shaded areas indicate when the input is permitted to change for predictable output performance.

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT :  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.16 Waveforms showing the set-up and hold times from the parallel load input ( $\overline{PL}$ ) to the data input ( $D_n$ ).



The shaded areas indicate when the input is permitted to change for predictable output performance.

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT :  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.17 Waveforms showing the set-up and hold times from the count enable and up/down inputs ( $\overline{CE}, \overline{U/D}$ ) to the clock (CP).

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".