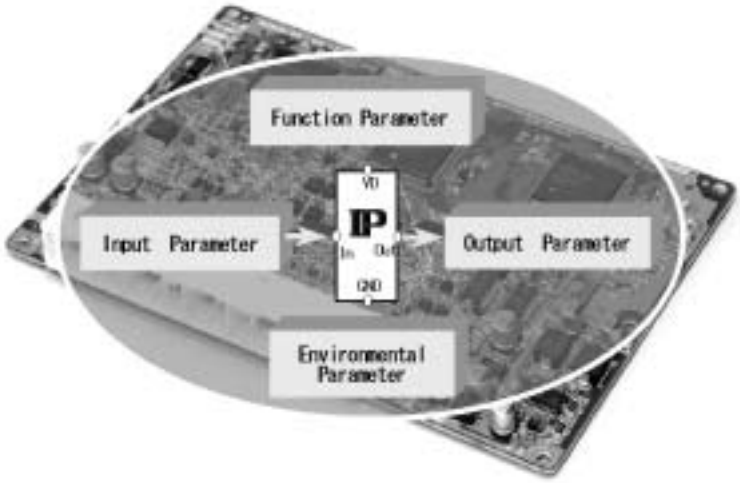
Creation of Intellectual Property for Hardware Designs

Akio Okahara
Syouhei Miwa
Syuuji Kimura



Abstract

To maintain growth amid a turbulently changing world situation, enterprises must move actively ahead with development of new business fields that accurately reflect market needs. It is important that the design outfits - who handle the initial phase of product development - reform their working method to one that emphasizes reuse of designs and hence achieve groundbreaking improvements in design efficiency and quality. In this way they will progressively propel large numbers of designers into new fields.

To that end it will be necessary to make good use of pre-designed and -verified reusable blocks of design outcomes (intellectual property - IP) in the product design arena as a means of raising design efficiency and quality.

This paper takes a close-up look at circuit design processes in the field of hardware design for in-vehicle control equipment. It describes the basic concepts for Circuit IP that are currently being created at our company and presents independently developed design support tools intended to facilitate effective utilization of such concepts.

1 Introduction

Automobiles and the automobile industry find themselves in a turbulently changing environment. Now and into the future the industry must accelerate its CO2 reduction for global warming prevention, as well as its reduction of pollutants of various kinds and its R&D for improvement of recycling rates. At the same time it will have to pursue R&D in response to the IT transformation that is bringing new capabilities for automobiles - in other words it will have to accommodate the "ubiquitous society."

To cope with such diversification of their R&D agendas, automobile manufacturers have been pursuing "modularization," "revision of R&D alliances" and similar programs to achieve higher efficiency of their R&D. But such efforts remain inadequate. With development based on conventional techniques, R&D is completed in a short time (heightening work efficiency), and the labor savings are shifted into new system (device and product) development.

2 Transformation of manufacturing at our company

2.1 Developments to date

An urgent task for our company as an automobile parts manufacturer, as for others in the industry, is to speedily implement a power shift, heightening development speed using conventional techniques, and implementing new development (with the savings in labor). To tackle that task we have been engaged in activities aimed at a "new manufacturing" for our enterprise. The first step was our SRM2000 (Super Rapid Module) endeavors which were launched in 1997. These were activities to optimize our operations from design and development through to manufacture of products, so as to shorten the duration of product development and drastically raise our cost competitiveness. They made use of concurrent engineering methods to have all engineers engaged in product design, evaluation and manufacture share all pertinent information and know-how in the product planning stage, so as to achieve early identification and resolution of problems and thereby realize optimization of the manufacture of each product. (Refer to Fig. 1.)

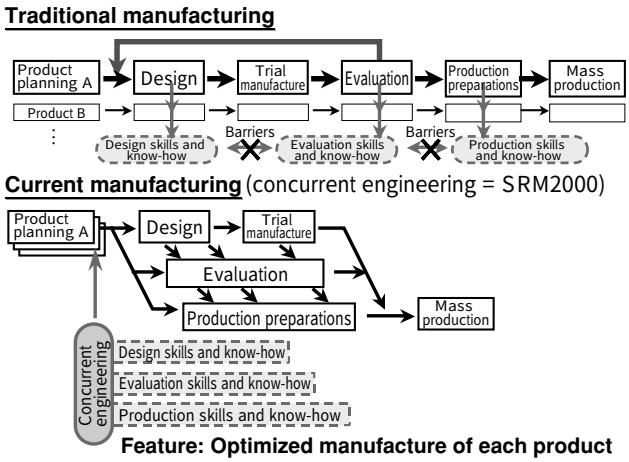


Fig.1 Transformation of manufacturing via SRM2000

But optimization of development of each product is inadequate by itself to cope with diversification of systems and increases in the volume of development. Rather, our operations must evolve into new forms of product development and manufacturing that achieve overall optimization encompassing our Group, its outfits, operations and enterprises as a whole.

Our SRE2001 (Speedy Reliable Engineering) activities were launched in 2000 as a means of realizing such overall optimization. These activities represent an attempt to optimize our operations as a whole by achieving harmonization and equalized, interlinked status among each of the individual operations of design, evaluation and manufacture, for a large number of products. Engineers who are successful in this attempt will be able to incorporate into the design, manufacturing or other work of their own particular fields the excellent design property and know-how, etc., that exists in the other fields and that they have hardly made use of hitherto. And by practicing such mutual reuse across numerous fields it will be possible to realize shortening of development durations and enhancement of quality. Moreover the individual operations of design, evaluation and manufacture will be optimized simultaneously with the progressive optimization of the overall flow of operations; thus it will be possible to achieve a globally optimized, new manufacturing. (Refer to Fig. 2.)

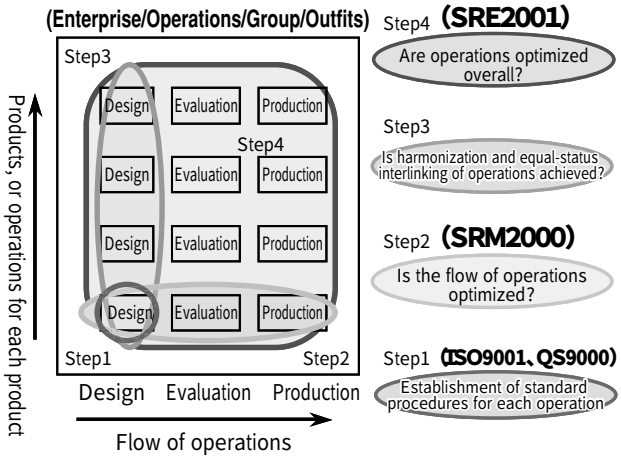


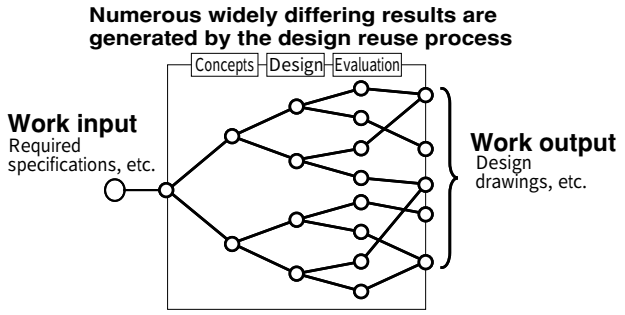
Fig.2 Overall optimization of operations (SRE2001)

An additional consideration is our company's ongoing pursuit of a fusion of the automotive electronics and car infotainment sections; in support of such pursuit it will be important to realize overall optimization encompassing each section at an early date.

2.2 Issues in design

A method of reusing design property that was employed in the past was for the designers to produce design outcomes (circuit diagrams and printed circuit board diagrams, etc.) for their respective products with optimization of the product as their major aim, then register such outcomes as standards available for reuse. But under this method insufficient attention was given to reuse during the initial stage of design, so that often no clear records were left of the ideas, thinking (principles), problems deliberated and results of such (constraints, etc) from the time when the design was made, although such information is of the highest importance when implementing reuse.

With this conventional method of standardization, error-free reuse of past design outcomes was not possible unless compilation of information concerning outcomes started with the individual designers themselves. But since each designer possesses different skills, different designers will produce different results for a given task. This is true even in cases where one assumes the outcome should be the same whoever performs the task. Given such a circumstance, no improvement in the quality of design could be hoped for. (Refer to Fig. 3.)



Conventional standardization method:

People are required to use something that someone else has determined.

⇒ " Black box "effects

⇒ Insufficient information to accommodate changes

⇒ Deficient quality of work and designs

Fig.3 Conventional method for standardized design and its problems for reuse

To break out of this impasse we have employed a method of more stringent checklists plus more stringent design review (below, "DR"), and have tolerated the increase in our design workload that it entails. But as the sole method of design quality improvement this is already reaching the limits of its ability to cope with the increasingly diverse systems and the expanding volume of development.

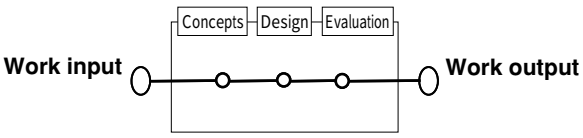
2.3 Realizing a new manufacturing

One of the most important means for realizing a new manufacturing is IP (intellectual property).

Switching to an IP modus operandi involves turning design ideas, thinking (principles), problems deliberated and verification results into document forms that are acceptable to anyone (that follow principles), and managing such documented design information in a unitary manner so that it can be reused.

Our company gives the following specific definition to the design IP to be used by its product design outfits: "Design property, such as requested specifications, design specifications and design results for individual function block units, which by being shared at the level of such units and by subsequently being reused in product design or in new IP design, can enable improvements in design quality and efficiency."

Thus, use of managed design IP will make it possible to eliminate the errors of judgment to which designers are liable when reusing design information, and to obtain results that conform to a single, appropriate set of principles. Further it will enable all of the designers to share the same objectives, which besides stabilizing and enhancing design quality will also permit a steady enhancement of design efficiency. (Refer to Fig. 4.)



IP methods:
- Materials that are understandable and acceptable to anyone are determined and used by all of the personnel according to appropriate principles.
- The " IP " shared intellectual property undergoes property management to promote continual rises in its value.

When the materials are turned into shared property, the objectives of all personnel involved in the operations come to coincide as a natural result.

⇒ The quality of the work and designs is stable.

Fig.4 Reuse under IP setup

And by progressively expanding the scope of the IP modus operandi to cover all technical information relating to manufacturing, our company will realize the overall optimization via new manufacturing (SRE2001) at which it is aiming. (Refer to Fig. 5.)

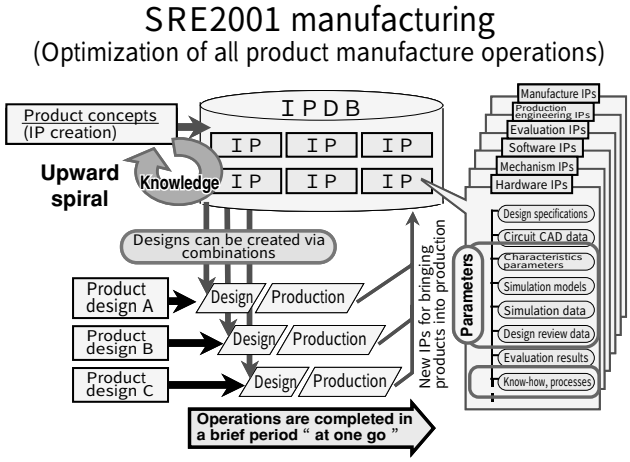


Fig.5 The new manufacturing (SRE2001)

Our company is proceeding with activities to introduce IP based on the above thinking to various design fields including hardware, mechanisms, software and production engineering. This paper focuses on circuit design - the very first stage in hardware design - and examines some crucial aspects of the introduction of Circuit IP.

The paper also introduces the proprietary IP design support tools that our company has developed in order to maximize the beneficial effects of Circuit IP when it is reused in product design.

3 What "Circuit IP" is

3.1 Principles of Circuit IP design

The first requirement for effective utilization of Circuit IP so as to achieve simultaneously the goals of improving the efficiency of product design and improving its quality, is to have a library of reusable Circuit IPs. But for such a library to be possible, Circuit IP developers must use consistent design methods that permit the creation of reusable Circuit IPs. Such methods must be based on the following principles:

①Prepare design information that takes into account that the Circuit IP content will be altered and reused by IP developers and other design teams, and provide such design information relating to each stage - specification design, constant design, printed circuit board design, product manufacture design and inspection.

②Use tools and design processes that permit incorporation of design information in consistent and easily communicable forms.

③Use tools and design processes that permit Circuit IPs to be connected together easily despite the absence of the original IP developer.

To meet these conditions it will be indispensable to perform design in conjunction with the IP design support tools that are presented in Section 4.

3.2 Design units for Circuit IP

In the electrical system CAD ("Design Synthesis" application) employed in conventional circuit design work, the unit for circuit design is the unit constituted by the printed circuit board. But taking printed circuit boards as the individual items (units) of IP would be inappropriate since the printed circuit board is too large a function unit for reuse by most other design projects and design teams; nearly all of the function/design materials of a board will be unsuitable for them to reuse. In the field of automotive electronics, in particular, the products in nearly all cases consist of a single printed circuit board which is composed of numerous function blocks (such as power supply circuits, circuits for interfacing with various sensors and actuators, microcomputer circuits, etc.) connected together. (Refer to Fig. 6.)

In the interest of ease of reuse, it is preferable that

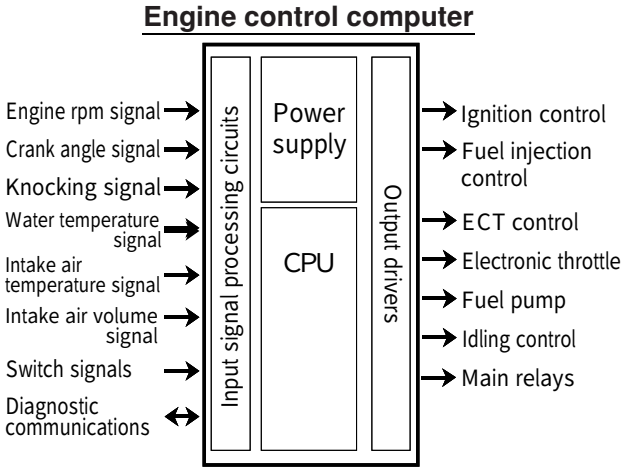


Fig.6 Sample configuration of engine control computer

the design units for Circuit IP should be the individual "function blocks" such as enumerated above. And to have Circuit IPs reused by large numbers of projects and design teams and hence bring about efficacious improvements in design quality and efficiency, the size of the function block units must be defined in advance. Naturally however, stringent limitations on the size of the function blocks will not be necessary.

Table 1 lists Circuit IP function block units that have been segmentalized and minimized for ease of reuse in the field of automotive electronics. Such function units are power supply circuits, circuits for interfacing with various sensors and actuators, microcomputer circuits, communication circuits, and so forth. Taking these 30 or so function blocks as the smallest function units for Circuit IP means that provided their specifications are congruent, Circuit IPs can be mutually reused among various different Electric Control Units (ECUs) in the field of automotive electronics.

Table 1 Smallest function units for Circuit IP

Input	Switch input circuits	Analog input circuits
	MPU input circuits	MRE Hall sensor input circuits
	Knocking input circuits	A/F input circuits
	Resolver input circuits	Automatic light control sensor
	High frequency input circuits	input circuits
Output	Small-signal output circuits	Valve relay output circuits
	Resolver output circuits	Lamp/heater drive circuits
	Small-signal analog output circuits	Airbag squib circuits
	Motor output	
	・H bridge circuits	・Stepper drive circuits
Serial communication		
	CAN communication circuits	Body system communication circuits
	Differential communication circuits	ISO9141 circuits
	Local communication circuits	
Sensors	Millimeter wave sensor	Acceleration sensor
	Torque sensor	
Other	Power supply circuits	CPU + peripheral circuits
	Capacitor memory circuits	EEPROM

Considered solely in terms of development of a given type of ECU (for example an airbag ECU or engine control ECU), combining several of the minimal function units described above to form an item of Circuit IP will be a valid practice. But one must consider the enterprise and its operations as a whole over the long term and bear in mind that developmental design is set to diversify in the future. One then sees that in order to distribute developmental resources within the area of developmental design in a manner concordant with overall optimization, and hence create a development setup achieving maximal efficiency, it will be absolutely necessary to design reusable Circuit IPs based on a viewpoint that transcends individual fields and to treat such Circuit IPs as shared property.

The ASIC development field is currently provided with fully adequate design tools. Estimates calculated for this field indicate that the cost of designing conventional reusable blocks is 2 to 3 times higher than the cost of designing blocks that are used only once. They also show however that employing blocks that are designed for high reuse capability will cut the labor required for development to 1/10 or less compared with that required to develop a once-only use block with the same functions. This means that reuse of such blocks will increase design productivity by a factor of 10 or more. By contrast, reusing blocks that are designed without adequate attention to reuse will raise productivity by no more than a factor of 2. Thus it is estimated that employing blocks that are designed for reuse will bring a five-fold or greater increase in productivity compared to employing blocks designed without attention to reuse.[1)]

3.3 Requisite information for Circuit IPs

There exist several conditions for designing completely reusable Circuit IPs. These conditions are described below.

①The Circuit IPs must be designed so as to offer solutions for a wide range of problems. That is, they must be readily alterable so that they can be applied in applications differing from that initially targeted by the design.

②Models must be provided that can be used for simulation with a wide variety of simulators.

③The Circuit IPs must be verified independently of the applications in which they are to be used. With some products or applications a Circuit IP will only be subjected to a partial verification that is specialized for the particular product or application, in order to avoid the trouble of developing a test bench for verifying all of the Circuit IP's functions. To assure reusable design therefore it will be necessary to provide simultaneously a method, provided at a higher level, for verification of the Circuit IP in isolation.

④The Circuit IPs must be verified such that high reliability is obtained. Contrary to condition (3), this condition requires that it be possible to verify Circuit IPs under simulation of the products or applications for which they will actually be reused. An example of how this condition may be met is pre-installing Circuit IP blocks in a Rapid Prototype ECU board such as featured in the CRAMAS Rtype real-time simulator developed by our company, which will permit easy verification of such blocks under conditions simulating the products or applications in which they will actually be used. It will additionally be necessary to provide information permitting verification of the parts layout and pattern connections on the printed circuit board, in tandem with a noise simulator or similar.

⑤The application ranges and constraints must be completely stipulated. The full range of parameters defining the Circuit IP's characteristics must be stipulated, together with effective methods for altering such parameters. Further, all constraints applying to such parameters and alteration methods must be quantitatively stipulated. Additionally, requirements for and constraints on interfaces figuring in the Circuit IP use methods must also be stipulated.

It is not of course the case that the Circuit IPs accumulated by our company to date meet all of these conditions. There remain many tasks to be undertaken before that can be achieved, among them perfecting the IP design support tools to be discussed in the following section, providing device models for the circuit simulator and validating the noise simulator.

The present subsection describes important aspects of the Circuit IP parameters devised by our automotive electronics outfits in order to meet condition ⑤ above, and the functions that such parameters are able to realize.

A Circuit IP is a block of circuits configured using several circuit elements such that it realizes at least one function. Such a circuit block may be considered as a basic entity (or some such thing) and will definitely include one or more input terminals, output terminals and power terminals. Quantifying the interrelationships between the voltage values or current values at the terminals of a Circuit IP constitutes the fundamental step in describing the Circuit IP's parameters. It is an operation that can be alternatively characterized as putting into clear document form the items which the circuit designer has to deliberate and determine as a matter of course.

All Circuit IP parameters can be assigned to one of the following four categories: function parameters, input parameters, output parameters and environmental parameters. (Refer to Fig. 7.)

Function parameters state the relationships between the voltage value(s) (or current value(s)) of the Circuit IP's input terminal(s) and those of its output terminal(s). In other words they give the functions that the Circuit IP possesses. The relationship between power supply voltage and power supply current is also expressed as a function parameter.

4 parameters for describing circuit performance

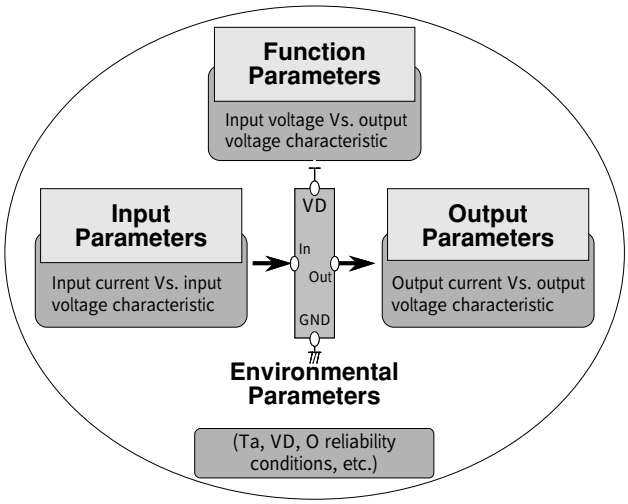


Fig.7 Categorization of Circuit IP parameters

Input parameters state the relationships between the voltage value(s) and current value(s) at the Circuit IP's input terminal(s). Input voltage limits, input current limits and so on are also expressed as input parameters. These parameters can be used to state interface information for the Circuit IP's input.

Output parameters state the relationships between the voltage value(s) and current value(s) at the Circuit IP's output terminal(s). Output current limits and so on are also expressed as output parameters. These parameters can be used to state interface information for the Circuit IP's output.

Environmental parameters state the application ranges, such as power supply voltage range and operating temperature range, that will guarantee the characteristics given by the Circuit IP's three other parameter categories, namely its function, input and output parameters.

Based on a consideration of their past experience and know-how, our automotive electronics outfits have compiled a set of guidelines on the items that should be included under the four parameter categories in the case of each of the aforementioned minimal function units for Circuit IP. Under these guidelines even a simple circuit block (Circuit IP) such as for example that in Fig. 8 will require verification of at least 13 parameters for reliable reuse. (Refer to Table 2.)

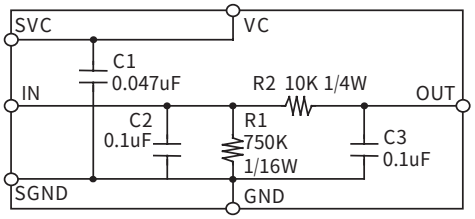


Fig.8 Sample analog input circuit

Table 2 Sample Circuit IP parameters

	Parameter	Symbol	Condition	Min	Typ	Max	Unit
Environmental	Operation assurance circuit ambient temperature	Toap		−40	25	+105	℃
	Operation assurance VD power voltage	VDop	Ta=full Taop range	−50	—	+50	V
Function, control	Vin-Vout characteristic gain	GAIN	Ta=full Taop range	0.9998	—	1	—
	Constants for output pulse rise	Tup1	Ta=full Taop range, load capacity CL≦1000 pF	0.70	1.00	1.34	ms
		Tup2	Ta=full Taop range, load capacity CL=0.01uF	0.79	1.10	1.44	ms
		Tup3	Ta=full Taop range, load capacity CL=0.1uF	1.63	2.00	2.40	ms
		Tup4	Ta=full Taop range, load capacity CL=1uF	10.0	11.0	12.0	ms
	Constants for output pulse fall	Tch1	Ta=full Taop range, load capacity CL≦1000pF	0.70	1.00	1.34	ms
		Tch2	Ta=full Taop range, load capacity CL=0.01uF	0.79	1.10	1.44	ms
		Tch3	Ta=full Taop range, load capacity CL=0.1uF	1.63	2.00	2.40	ms
		Tch4	Ta=full Taop range, load capacity CL=1uF	10.0	11.0	12.0	ms
	Gain frequency characteristics	GAIN1	Ta=full Taop range, load capacity CL=open, frequency=100Hz	−2.31	−1.45	−0.77	dB
		GAIN2	Ta=full Taop range, load capacity CL=open, frequency=10KHz	−38.5	−34.0	−32.8	dB
		GAIN3	Ta=full Taop range, load capacity CL=open, frequency=1MHz	−78.5	−76.0	−72.8	dB
Input	Vin input current coefficient	KIp	Ta=full Taop range	9.371	9.868	10.364	KΩ
	Vin ground voltage coefficient	KGp	Ta=full Taop range	0.0119	0.0132	0.0148	—
	Vin output voltage coefficient	Kop	Ta=full Taop range	0.9852	0.9868	0.9881	—
	Input maximum rated voltage	Vinmax	Ta=full Taop range, | Vin-Vout | <50V	−50	—	50	V
	VD power current consumption	Id	Ta=full Taop range, VD=50V, VGND=0V, Isvc=0A	0	—	5	nA
Output	Vout output current coefficient	Kiout	Ta=full Taop range	9.496	10.000	10.502	KΩ
	Output maximum rated voltage	Voutmax	Ta=full Taop range, | Vin-Vout | <50V	−50	—	50	V

Clarifying the characteristic values given by the parameters constitutes the "specification design" of a Circuit IP, while quantifying the parameters' relationships with the characteristics of the elements contained in the Circuit IP amounts to implementing the "constants design." At the same time the parameters also represent, just as they are, the "inspection specifications" for verifying the Circuit IP in isolation. Making design revolve around the Circuit IP parameters in this way is an effective means for communicating the design intents via consistent descriptions.

3.4 Beneficial effects of parameter quantification

Fig. 9 shows an example of how the connection of 2 Circuit IPs is verified. The battery voltage VB, of the output parameter of circuit IP on the output side (VB-Output H Level Vout characteristics), and the input parameter of the circuit IP on the input side (VB-H level determination thresholds), is used as a common parameter for this verification, to derive the operating power voltage limit value.

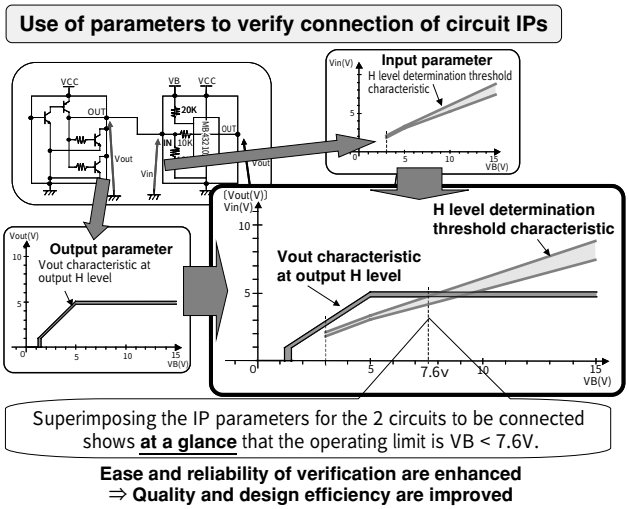


Fig.9 Sample verification of circuit connection via IP parameters

As this example shows, it is possible to verify the operating characteristics resulting from a wide variety of circuit connections simply by superimposing on one another the parameters (parameter graphs) concerned. Thus the use of parameters permits improved ease and reliability of verification and makes it possible to raise design efficiency and quality.

4 Development of IP support tools

4.1 Aims of the development

Further requirements for utilization of the IPs described above in product design are sound management of the IPs and heightened efficiency of their reuse. To meet those requirements we opted for a design operation flow of the kind described below, developed design support tools to support such operation flow, and engineered an environment permitting such tools to be used on the designers' PCs connected to the company-internal LAN.

4.1.1 Operation flow for the IP preparation and registration stages

①Designer designs the IP (provisionally registers the design documents into the database according to sequence)
②Application for IP registration is lodged with IP committee
③IP committee deliberates the application
④IP manager formally registers the items into the database

4.1.2 Operation flow for the IP reuse stage

①Conceptual design of the matrix product
②Preparation of a list of IPs for use in the matrix product
③Circuits are designed from the IP list via electrical system CAD
④Design information is consulted and design is checked, etc., through links to the IP database established via the electrical system CAD
⑤After passing DR, the matrix circuits are approved
⑥Design of target circuits
⑦After passing DR, the target circuits are approved
⑧Flow moves on to the printed circuit board design operations

4.2 Overview of the support tools (description of functions)

4.2.1 IP design support database

This has been developed so as to permit the use of functions for IP preparation, consultation and management, plus functions for preparing IP lists for use with individual products, via a browser. (Refer to Fig. 10.)

Fig.10 IP Design Support Database

①IP preparation (supporting ① of 4.1.1)

Data of the following kinds can be registered in the database to facilitate efficient implementation of reuse design employing IP:

・Category keywords (for circuit block categories, overviews, etc)

・Design specifications (including parameters)
・Circuit diagrams (CAD data are discussed later)
・Technical standards to be used in design
・Models and environment setting files for simulations
・Evaluation reports Etc.

②IP management (supporting ②, ③ and ④ of 4.1.1)

Since IP is liable to vary with the preparation circumstances and is subject to changes after registration*, functions of the following kinds are provided for its management:

* When they are registered, IPs are of a level that will permit reuse but are not yet completed and await further enhancement of their value.

・Management of numbers of versions
・Indication of improvement level and registration status
・Work flow, from application for registration and deliberation of such through to registration

③Preparation of IP lists for individual products (supporting ② of 4.1.2)

After completion of conceptual design, functions including those listed below permit utilization of the specifications and IP category keywords to accurately and efficiently extract those IPs that conform to the specifications, in preparation for circuit design.

・IP search
・Consultation of registered IP information
・Preparation of IP lists for products
・Printing of product IP list files
・Registration (protected) of product IP lists

4.2.2 Accommodation of IP design by electrical system CAD

The functions described below have been developed and added to the Design Synthesis application of the electrical system CAD used by our company, so that design using IP can be implemented efficiently on such application. (Refer to Fig. 11.)

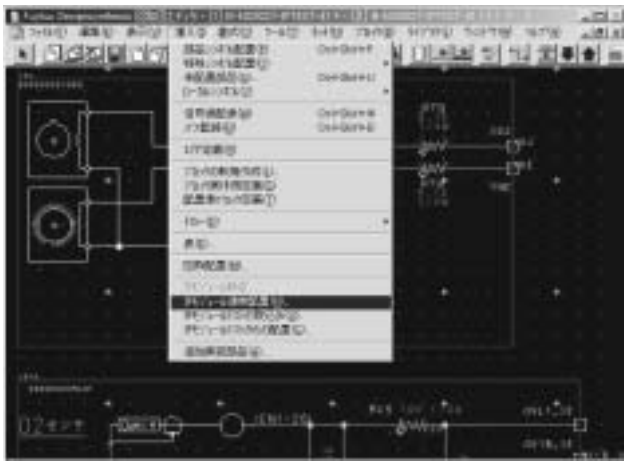


Fig.11 Electric CAD functions accommodating IP design

①IP circuit preparation (supporting ① of 4.1.1)

These are functions for preparing and registering in advance the circuit blocks that are to be managed as IP, in the same way as with a parts library. They almost completely support standard CAD circuit edit functions.

These preparation functions additionally include items specific to IP, namely functions that can (a) provide IP frames that enclose IPs so as to clarify their extent both perceptually and in terms of data; and (b) (following deployment of IPs in circuit diagrams) provide dedicated terminals permitting connection with IP frame-external signals.

These IP circuit preparation functions can only be utilized by IP managers. General users are able to use only the functions in the remaining items below.

②Product circuit design (supporting ③ of 4.1.2)

These functions permit circuit blocks corresponding to particular IPs to be called up from IP list files and deployed in circuits (circuit diagrams). They are configured so that it is not possible for basic circuit information such as types of parts and signal connections within IPs to be altered on the circuit diagrams. Information that has nothing to do with circuit performance - such as part numbers and comments - can however be edited.

③Accessing information in IP database via IPs on circuit diagrams (supporting ④ of 4.1.2)

IPs on circuit diagrams contain links to the IP database, permitting access of the database for detailed consultation of IP design specifications and other items during DR of circuit designs.

④Other

The above IP design accommodating functions are proprietary to our company. Out of consideration for utilization of circuit data in subsequent processing and similar situations however, we have taken care to ensure that it will be possible to use standard Design Synthesis to run content checks of IP design circuit diagrams and utilize the data contained in them, etc., just as with other circuit diagrams hitherto.

4.3 Future goals

Many other functions besides those listed above will be necessary in order to use IP design as a support tool. In the present development we have created the minimal environment that will permit design using IP to begin (and that will provide important functions for management and efficiency enhancement). Development will be continued in the future so as to progressively improve this design environment. Some of the proposed improvements for the environment architecture are given below.

①Data linkage with PDM and other tools

Examples: ・Linkage with QC data for products using IP or related parts
・Close linkage with CAD and simulation

②Inter-IP circuit function checks

Example: ・Consistency checks of IN/OUT electrical

characteristics using circuits' IP parameters

③Linkage with IPs other than circuits

Examples: ・Timely advice messages on printed circuit board CAD regarding board design concern items arising from circuit characteristics
・Linkage between IPs (electrical parts) requiring heat dissipation and mechanical IPs via thermal design tools, for optimal design support

5 Future endeavors

Extremely large amounts of investment (labor) must be input before the beneficial effects of IP can be obtained. Investment is required to render the individual function blocks reusable so as to effect the switch to IP methods. And investment is necessary to develop the parameters that will permit expansion of the application range of Circuit IPs currently reusable only in circuit design, and permit quantitative verification of connection to IPs in other fields (such as printed circuit board, manufacturing/inspection, software and mechanism IPs). Furthermore, we will have to steadily accumulate design IPs in order to recoup such investments within a short period and to achieve major strides ahead in the future.

Converting all function blocks to IP at the same high level will not by any means yield solutions to the problems posed. Rather, different IP conversion levels must be used for different function blocks, according to accurate determination of the number of times that each function block will be reused and its range of application (IP availability).

With IP circuits that will be reused only one or two times for instance, it should suffice simply to provide the design specifications and as much evaluation result information as possible via the IP database, without making any detailed description of the parameters.

Similarly with circuits that will be reused numerous times but have a relatively fixed application range (such as ICs exclusively for engine control ECUs), it will not be necessary to describe the parameters in detail. For IP conversion of such circuits, describing clearly the circuit switching methods for each specification concerned (by means of a breakdown of the different cases involved) should make for adequate facility of reuse. Naturally it will also be necessary to provide a full set of circuit design specifications and evaluation result information, etc., for such circuits via the IP database.

Finally there are circuits (such as power supply circuits and communication circuits) that will be reused any number of times with many and various equipment types. The parameters for such circuits must be quantitatively described from the initial design stage onward. By so doing it should be possible to raise to the maximum the circuits' productivity when reused. In this way, one will have to proceed with activities to build up an effective stock of such properties while making a trade-off between the labor (investment) that is put into IP design and the beneficial effects that are obtained from the switch to IP methods.

6 Conclusion

The employment of IP-based design promises to yield extremely large improvements in design efficiency and quality. We are confident that this transformation (paradigm shift in design operations) will play an indispensable role in achieving the targets our company has set in its VISION2010 program. (Those targets are to be rated No. 1 supplier by our customers and to double our efficiency and growth.)

With effective design tools and step-by-step perseverant efforts on the part of the company's designers (who include the present authors), a five-fold efficiency increase such as achieved in ASIC development will not be beyond our reach in the future.

Cited reference

1)Michael Keating and Pierre Bricaud, Reuse Methodology Manual, Maruzen Co., Ltd., 2000.

Profiles of Writers

Akio Okahara

Entered the company in 1986. Since then, has been involved in engine control ECU development.
Currently the Expert of the 1st V.C Engineering Department of Vehicle Controller Division, Business Division Group.

Syouhei Miwa

Entered the company in 1982. Since then, has been involved in engine control ECU and design support tool development.
Currently the Manager of the Automotive Engineering Department of Vehicle Controller Division, Business Division Group.

Syuuji Kimura

Entered the company in 1982. Since then, has been involved in engine control ECU development.
Currently the Department General Manager of the 1st V.C Engineering Department of Vehicle Controller Division, Business Division Group.