CSD. P5. Analysis of circuits based on flip-flops and logic gates. Correction and feedback checklist

==========

- [ ] My analysis report is organised in sections. In order to save study time and generate useful materials I will work in group and ask questions.
- [ ] The key for writing reports: does my report have enough quality to be used as study material for preparing exams and discussing with other students? Can I present my project for a large audience?

1. **Specifications**

- [ ] My report includes specifications, solutions may be planned.
- [ ] Initial driving signals? What do they mean?
- [ ] How are you going to generate the CLK and other control signals for testbenches?
- [ ] Circuit drawn, not simply pasted from *digsys*.
- [ ] Use this activity to learn the basic theory behind flip-flops. What are the flip-flops used for? What is the difference between CD and K or between SD and J?
- [ ] What is the FF function table? What is the idea of sampled values in order to use it?
- [ ] How many CLK signals does the circuit have? Is it asynchronous or synchronous?
- [ ] Do not include materials from the internet not clear or not contextualised.
- [ ] I can find similar projects or tutorials in *digsys* to study and learn.
- [ ] If you are reviewing “theory” material, it can be placed in specifications or be annexed.

2. **Planning**

- [ ] My report includes the planning of the activity. So, it can be developed.
- [ ] The planning is clear, a sequence of operations. Each planned operation needs to be converted into some kind of development results.
- [ ] Planning steps are included to tackle complicated projects.
- [ ] If this is your first activity. Your initial step may be the analysis of a single flip-flop.
- [ ] Do I have questions on *digsys* tutorials examples?
- [ ] In which way we are going to organise this project in group?

3. **Development** to deduce timing diagrams and comprehend flip-flop operations

- [ ] Vertical time lines on CLKs’ rising edges. Without these time lines it is impossible to know how it works or may be analysed.
- [ ] Sampled values (coloured dots) on control signals? Without them it is impossible to apply the flip-flop function table.
- [ ] Timing diagram drawing has the minimum quality required (similar to other examples in *digsys*)
- [ ] Output vector values are represented; better use decimal or hexadecimal codes to compare solutions.
- [ ] The timing diagram contains annotations and discussion. It is meaningful and will be easy to use when comparing solutions from other methods.

4. **Testing** with other methods

- [ ] I’m indicating how the solution will be tested.
- [ ] How to capture the circuit using method II (Proteus) or method III (VHDL)?
- [ ] Proteus pictures are not too small or too big, making them impossible to correct.
- [ ] My report does not contain copy materials without acknowledgement (if you are discussing the project with other students, you must name them).
- [ ] The VHDL files are not invented, all names, signals,and circuits are translated from the plan.
- [ ] I know and have learned how to implement VHDL processes for periodic signals (CLK) and pulses (CD).
- [ ] Timing diagram pictures are not too small.
- [ ] All my timing diagrams contain comments and handwritten annotations.
- [ ] My prints do not contain black background (it is not allowed and I will save ink).
- [ ] The default vertical grid in ModelSim timing diagrams is removed, only my vertical time lines of interest are drawn.
- [ ] The RTL is checked and discussed before using ModelSim.