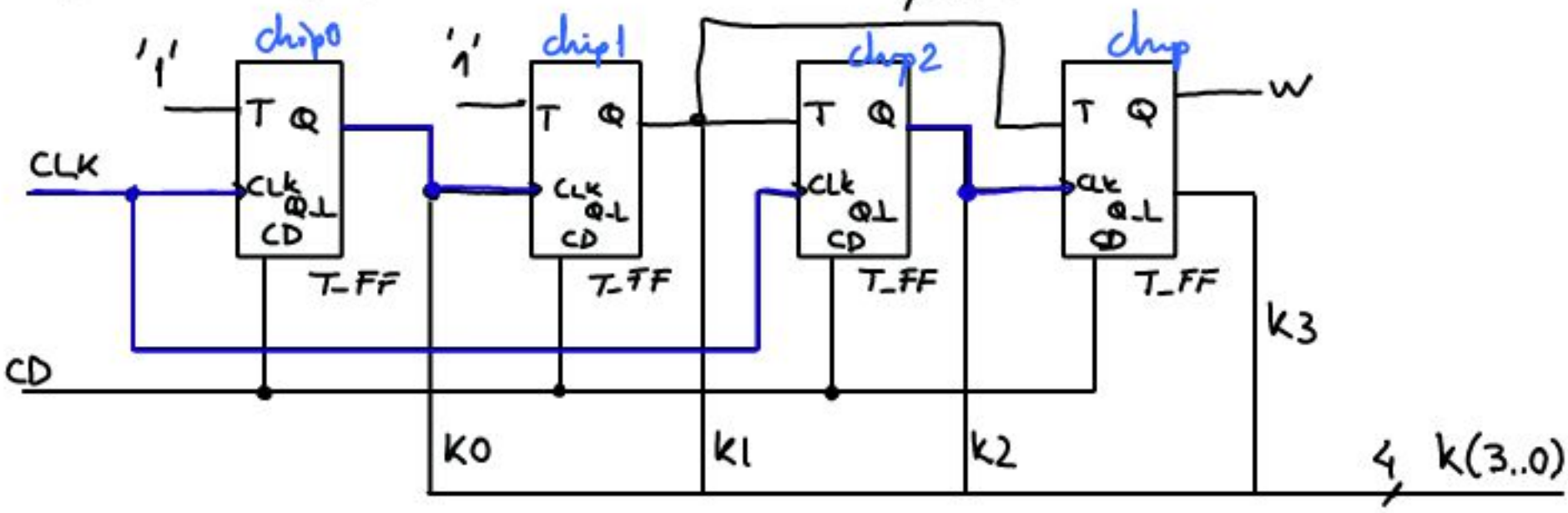
Example of commented solution

This is the circuit to be analysed

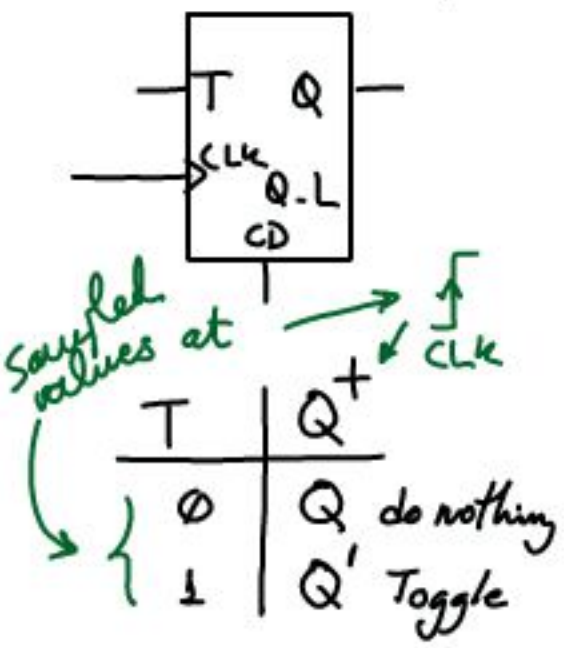


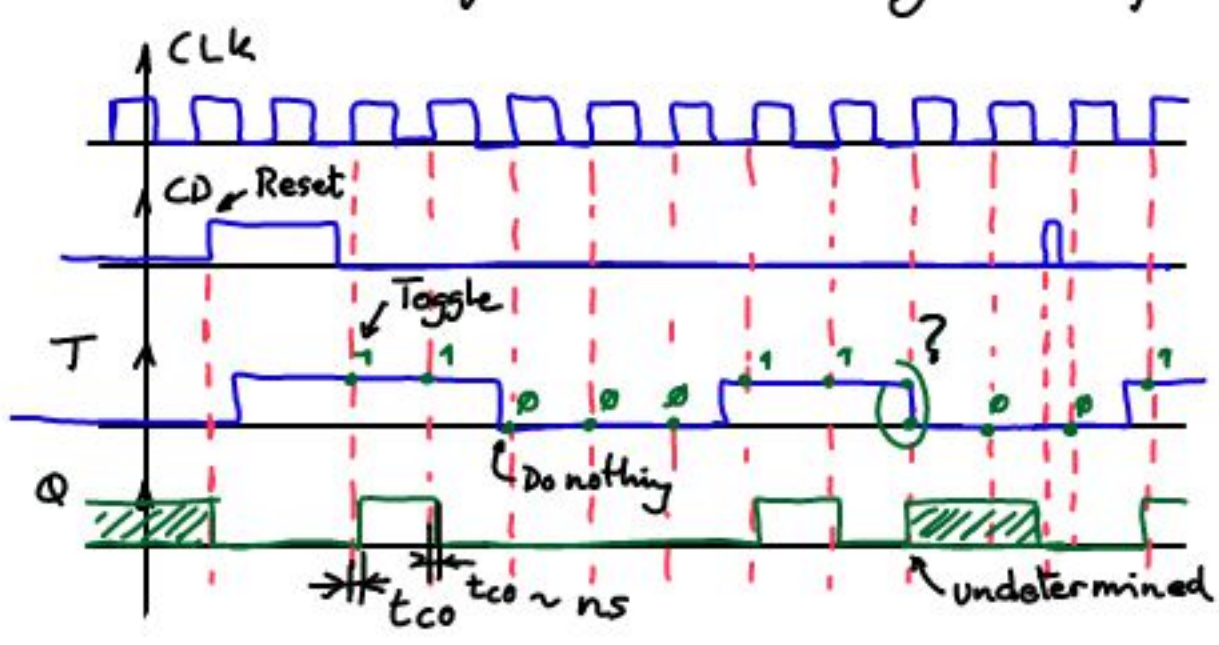
- 3 CLK signals to drive the FF → asynchronous circuit
- The circuit uses T_FF outputs to generate CLK signals

A possible plan to study how the circuit works may be:

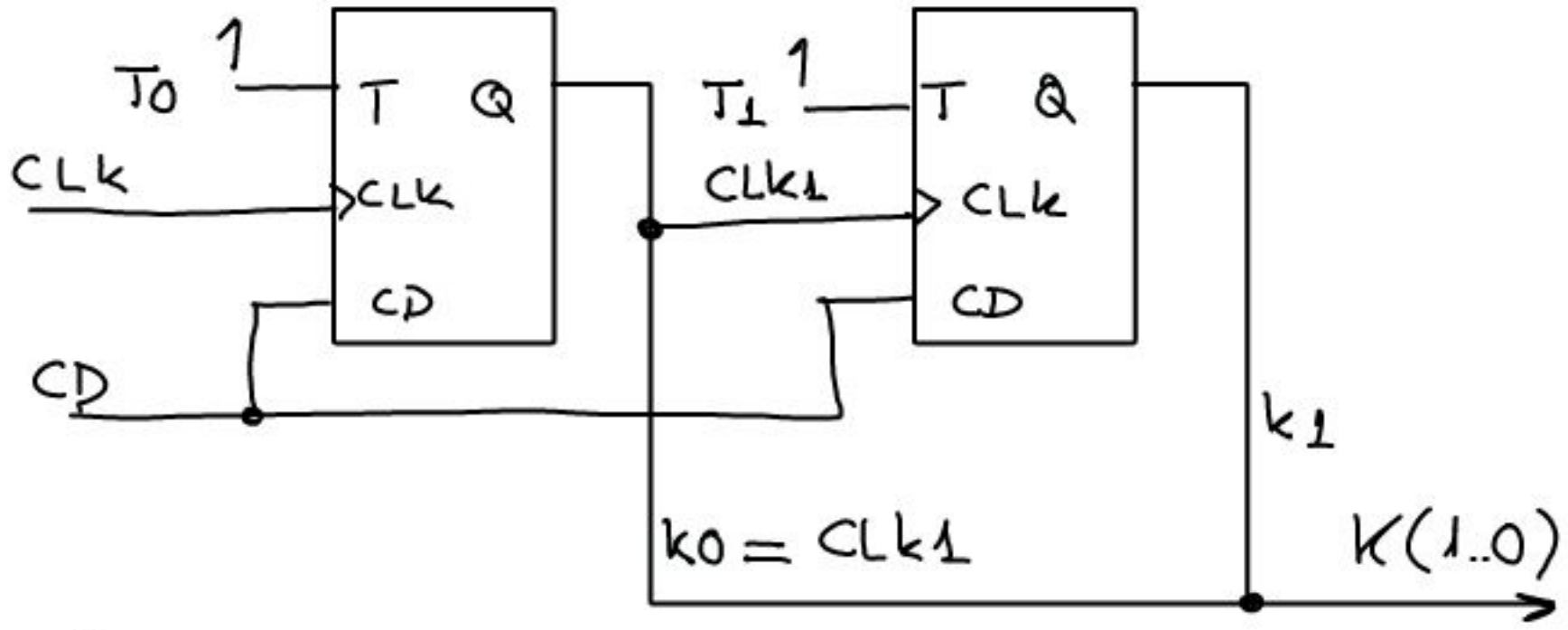
1. Study how a simple T_FF works
2. How to handle a circuit with 2 CLK's like the Chip0 and the Chip1 ?
3. Complete the analysis by means of a timing diagram
4. Determine how many states does the circuit have
5. Is there a better way to design an equivalent circuit? (for instance, as a FSM in P6).

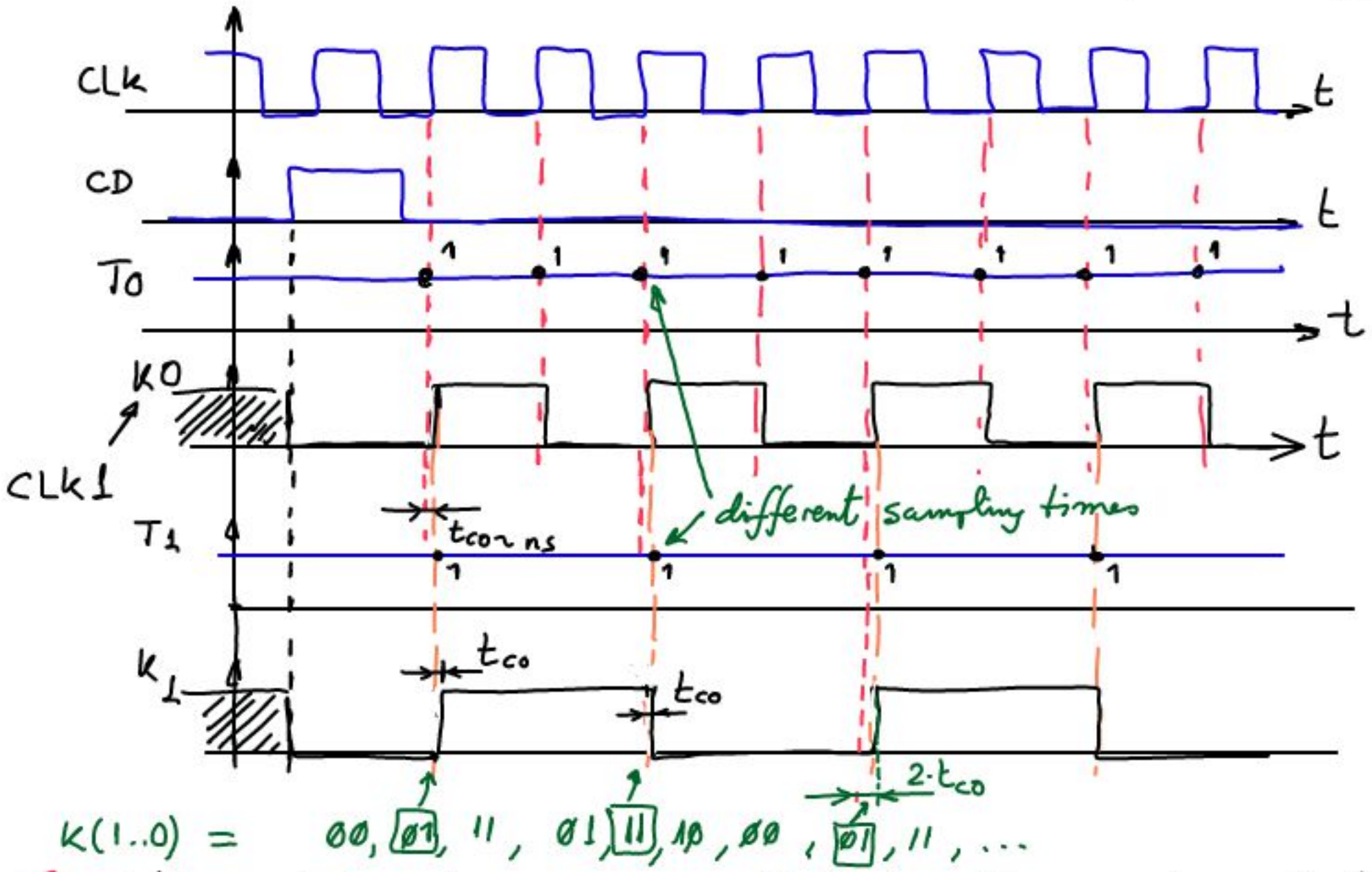
1. Let's analyse a simple T_FF for some T signal input ⇒ P5





2. Let's discuss how a system with 2 CLK's can be analysed





K(1..0) = 00, 01, 11, 01, 11, 10, 00, 01, 11, ...

Setting output values after multiple tco delays will complicate the circuits and make them very unreliable

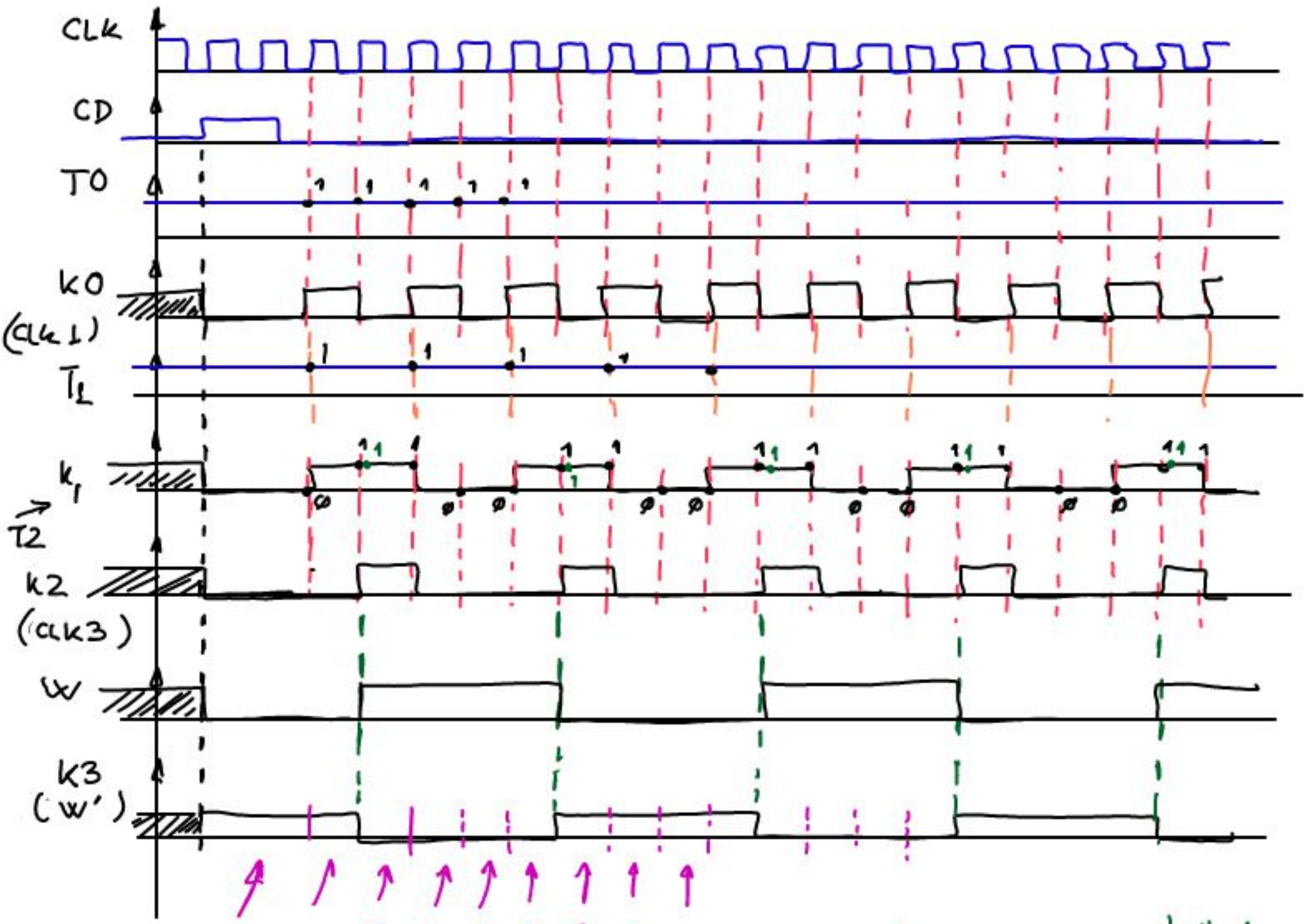
→ undesirable states in transitions

real output

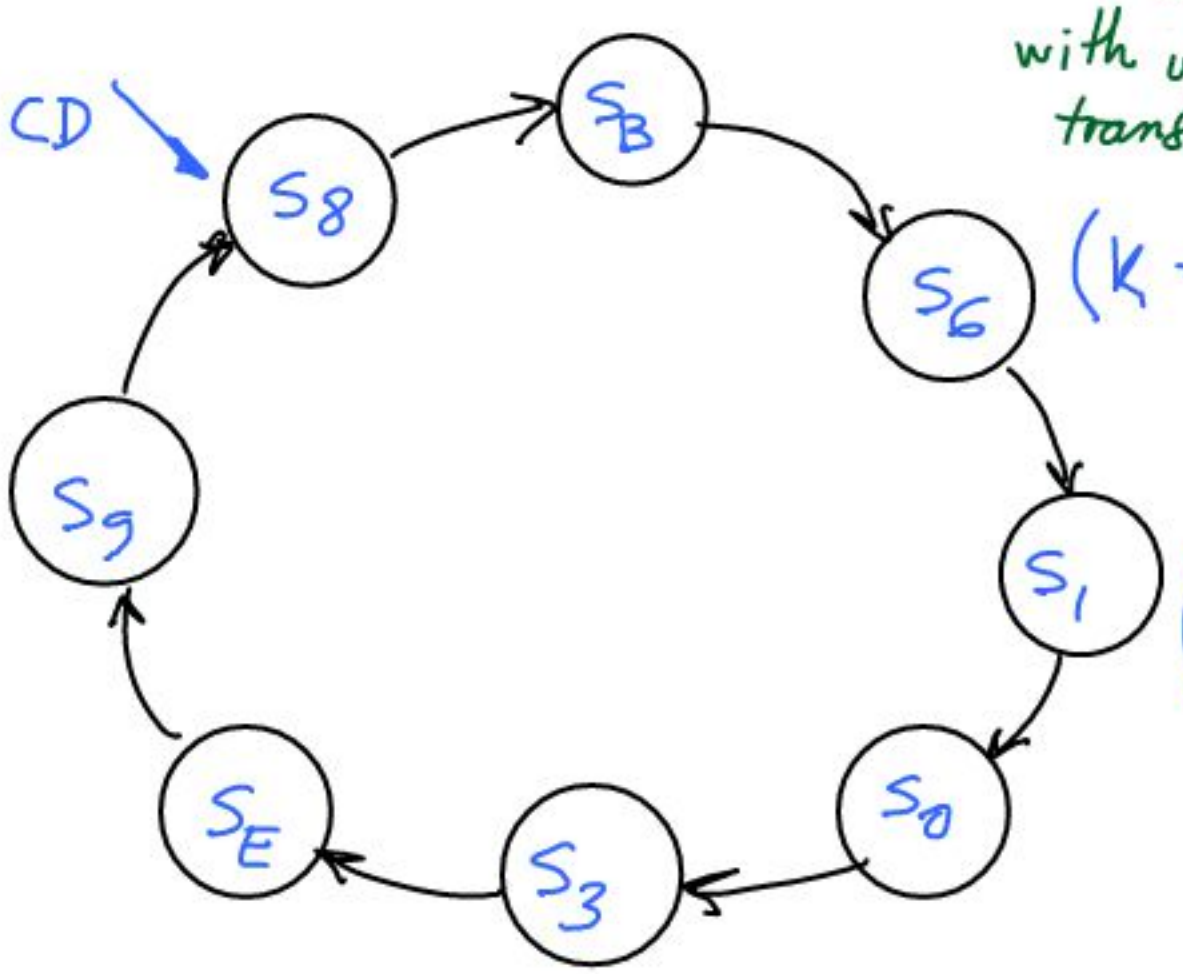
K(1..0) = 00, 11, 10, 10, 00, ... ← Ideal output

⇒ If k_1 is a $\left(\frac{f_{CLK}}{4}\right)$ output, it goes with a delay of $2 \cdot t_{co}$!! (bad design)

3. Therefore, with the previous analysis, we can try now the complete circuit, paying attention to the evolution of the CLK's



K(3..0) = 8, B, 6, 1, 0, 3, E, 9, 8, ... → This is an uncontrolled counter with 8 states with undesiable states in transitions



(K = Ø11Ø)

(K = ØØØ1)

Better design it as a FSM in P6