## EETAC - CSD



## **LAB 4.2 CONTROL SHEET**

			Date:
Grou	uр : G		
Stude	lent names:		-
			-
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Pre-la	lab activities (Check 🗸 if done)		
	#1. Truth table, timing diagram, input vect	tors, operations, etc.	
	#2. Quartus Prime project.		
	#3. Functional simulation.		
	#4. Timing analyser.		
	#5. FPGA pin assignment.		
	#6. Install the WaveForms software		
Lab a	activities (Check 🗸 if done)		
	A. USB-blaster driver		
	B. Programmer tool		
	C. Run the circuit and test operations		
	D. Static power consumption		
	E. Propagation delay		
	F. Dynamic power consumption		

Post lab assignment <u>PLA4</u>. Its due date is indicated in our <u>planning</u>.





Additional notes: