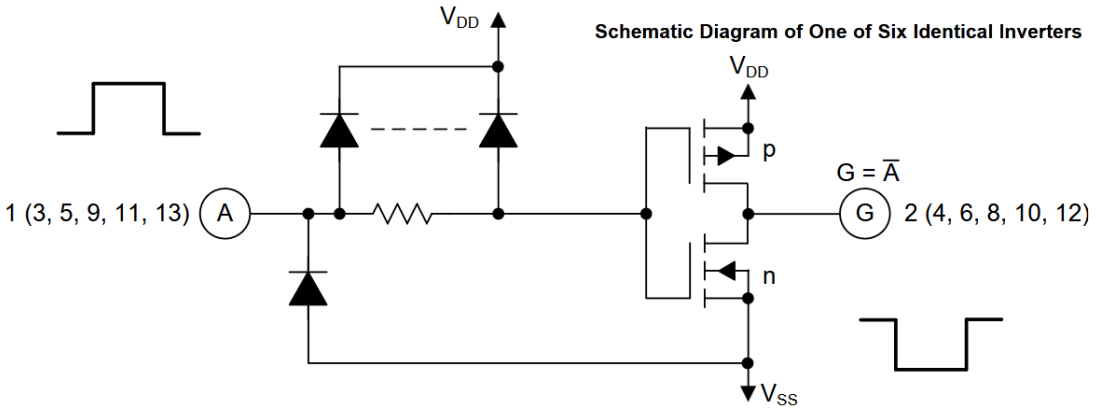
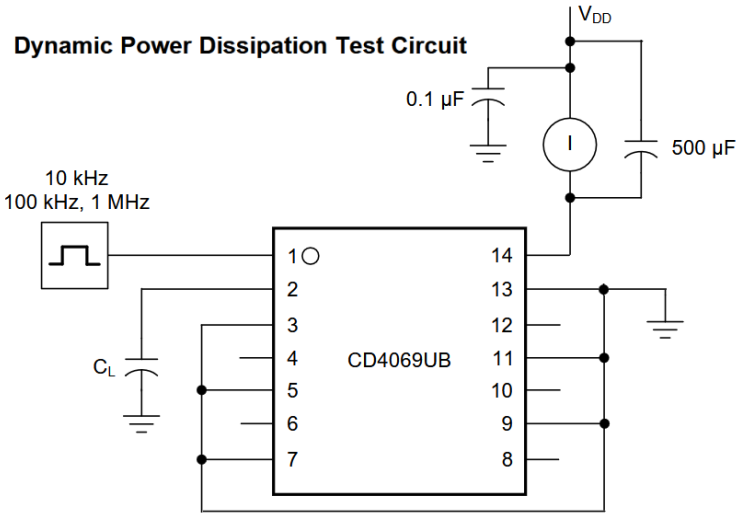
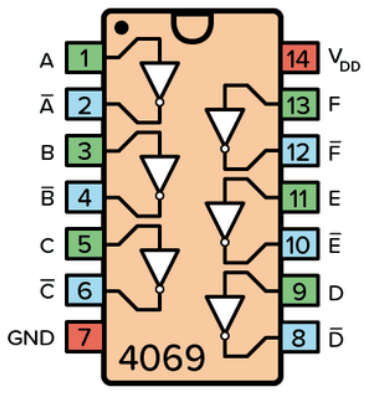
Lectures L1.6–L4.3: Electrical characteristics of a NOT logic gate in classic CMOS technology (V_{DD} = 5 V).

MC14069UB	Symbol	25°C			Unit
		Min	Typ	Max	
Output Voltage V_{in} = V_{DD} "0" Level	V_{OL}	—	0	0.05	Vdc
V_{in} = 0 "1" Level	V_{OH}	4.95	5.0	—	Vdc
Input Voltage "0" Level (V_O = 4.5 Vdc)	V_{IL}	—	2.25	1.0	Vdc
"1" Level (V_O = 0.5 Vdc)	V_{IH}	4.0	2.75	—	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	– 2.4	– 4.2	—	mAdc
(V_{OH} = 4.6 Vdc)		– 0.51	– 0.88	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	0.51	0.88	—	mAdc
Input Current	I_{in}	—	±0.00001	± 0.1	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	5.0	7.5	pF
Quiescent Current (Per Gate)	I_{DD}	—	0.084	42	nAdc
Total Supply Current (C_L = 50 pF) (Dynamic plus Quiescent (Per Gate)	I_T	I_T = (0.3 µA/kHz) f + I_{DD}			µAdc
Propagation Delay Times (C_L = 50 pF) t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 20 ns	t_{PLH}, t_{PHL}	—	65	125	ns







$$P_S + P_{dyn} = I_{DDQ} \cdot V_{DD} + V_{DD}^2 \cdot C_L \cdot f$$

Electrical characteristics of a NOT logic gate in LS-TTL technology.

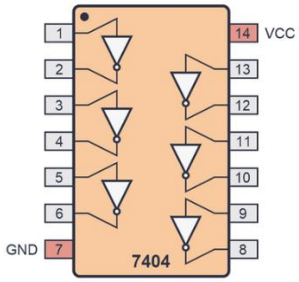
Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			–0.4	mA
I_{OL}	LOW Level Output Current			8	mA

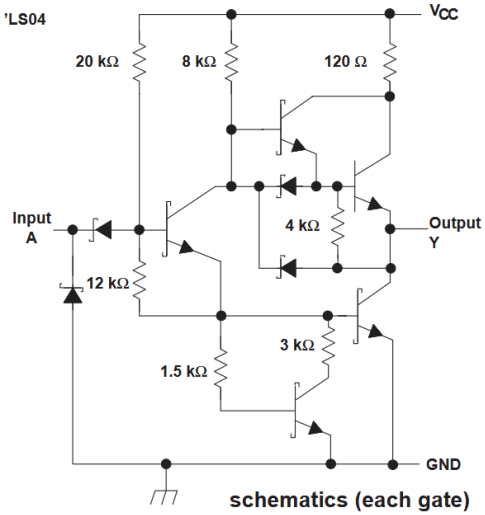
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Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = –18 mA			–1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			–0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	–20		–100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		1.2	2.4	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		3.6	6.6	mA

Symbol	Parameter C_L = 50 pF	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	4	15	ns





schematics (each gate)

