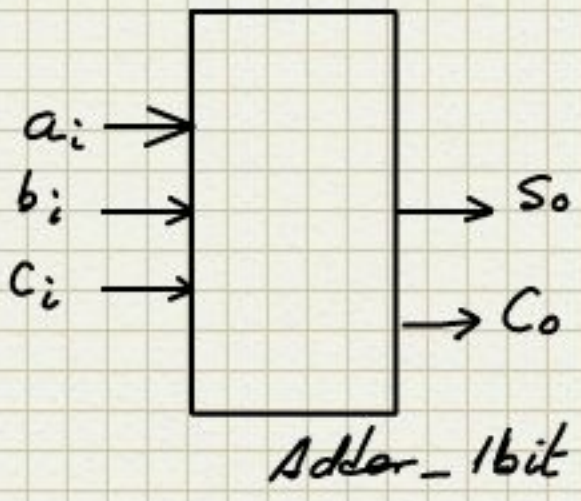
Example of the method of multiplexers

1. Specifications of the project: Design a 1-bit adder using the method of multiplexers and a MUX_4.



a_i	b_i	C_i	C_o	S_o
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(More sheets of paper are required as theory here in this especification if this is the first time you solve a circuit using this methodology)

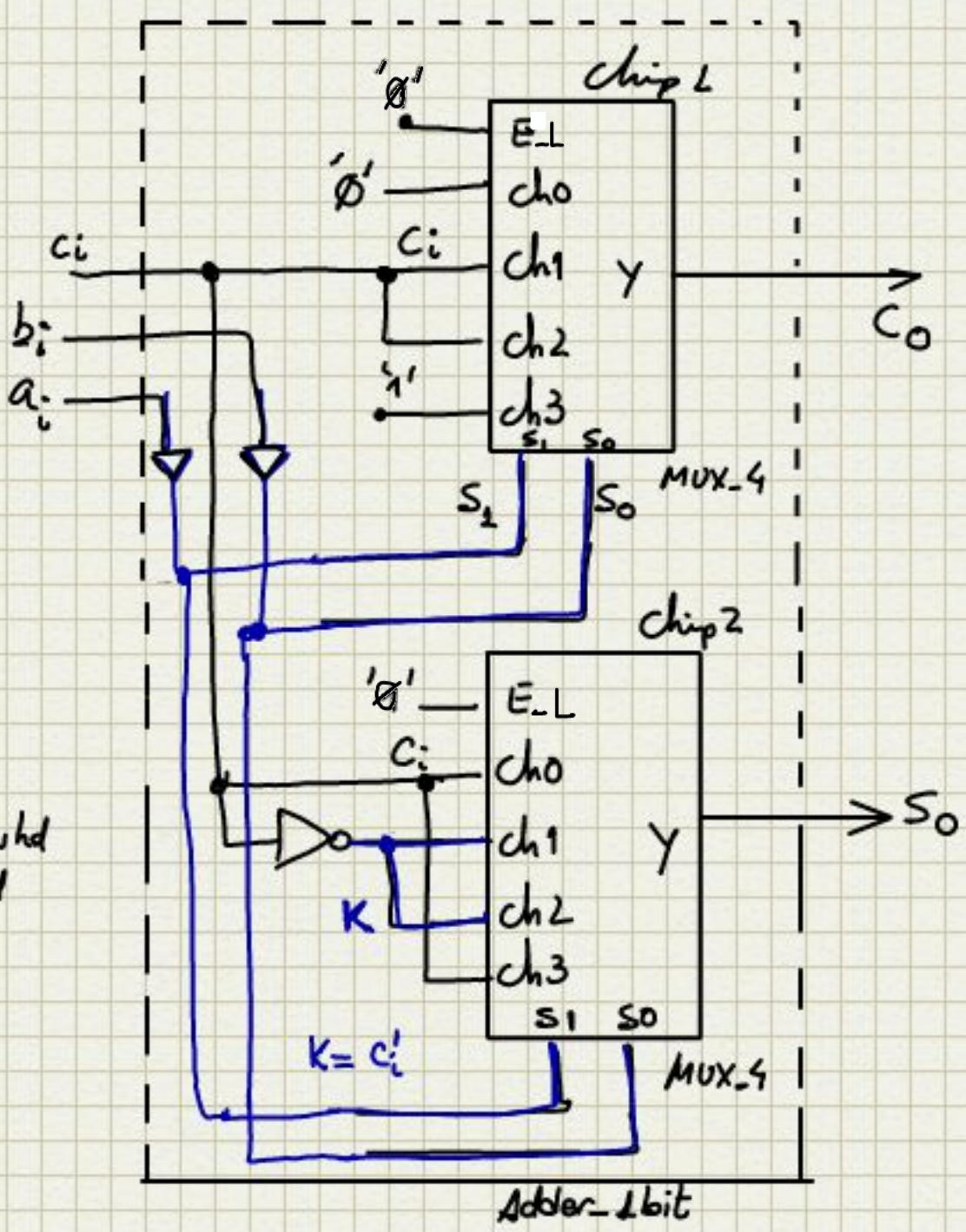
The theory on the method:
http://digsys.upc.es/csd/P03/P3_T/MUX/Method_of_mux.pdf

2. Plan

Let's analyse the thuth table considering that our MUX_4 will divide it into 4 sections corresponding to each channel

	a_i	b_i	c_i	C_o	S_o
ch0	0	0	0	0	0
	0	0	1	0	1
ch1	0	1	0	0	1
	0	1	1	1	0
ch2	1	0	0	0	1
	1	0	1	1	0
ch3	1	1	0	1	0
	1	1	1	1	1

S(1) S(0)



- Project of 2 VHDL files { Adder_1bit.vhd, MUX_4.vhd }

Let's define the project location

L:\CSD\P3\Adder_1bit_MUX4\

Project name Adder_1bit_prj

Find the schematic translation to VHDL in the web (P3).