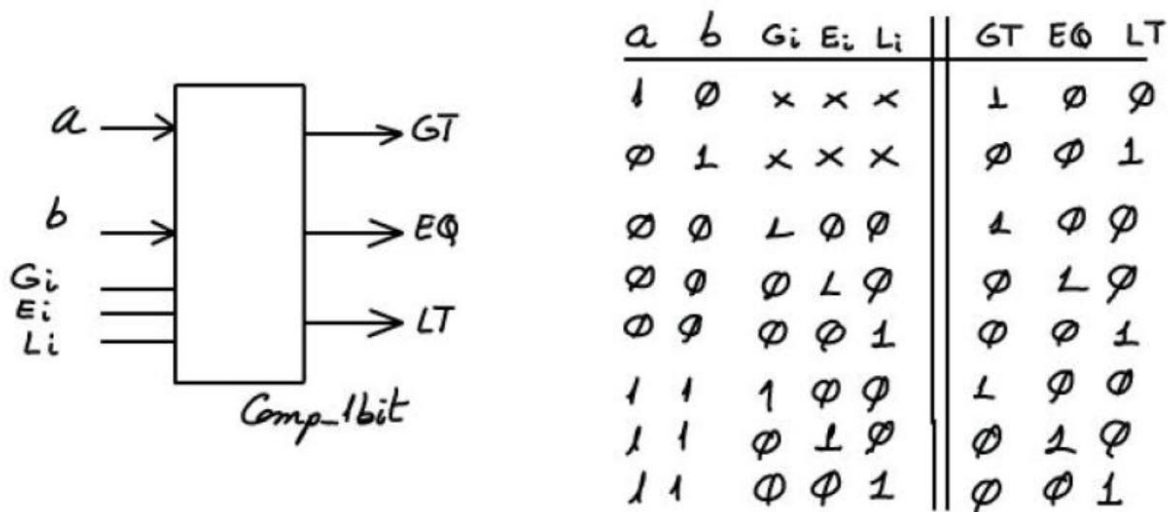


L3.1 activity #2 . Discuss and explain the questions



Specifications

1. Complete the *Comp_1bit* truth table

Planning

2. **Plan A** Describe the output $EQ = f(a, b, G_i, E_i, L_i)$ using minterms
3. **Plan A** How many maxterms include $GT = f(a, b, G_i, E_i, L_i)$?
4. **Plan B** Draw an example flowchart ready for translating the truth table into VHDL

Development

5. The RTL schematic is always the same, whatever the plan proposed to design the circuit. True or false?
6. The technology view depends on the target chip. True or false?

Testing and verification

7. Draw the testbench fixture schematic
8. How long will it take to test all the truth table if $Min\_Pulse = 1.23 \mu s$?