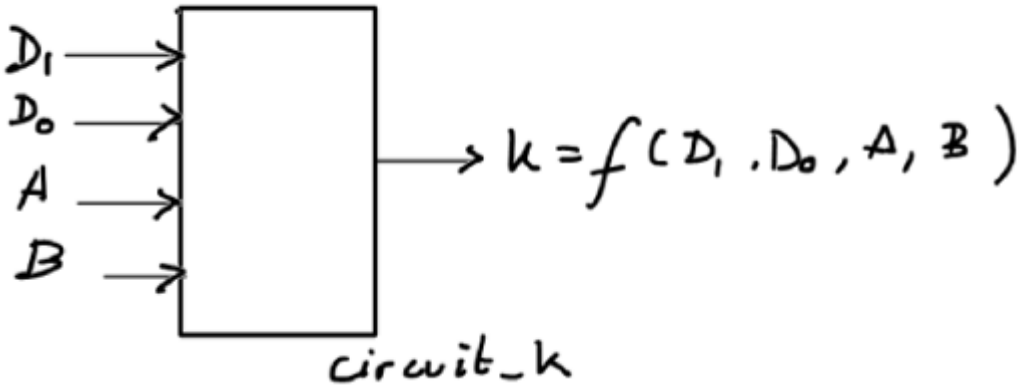
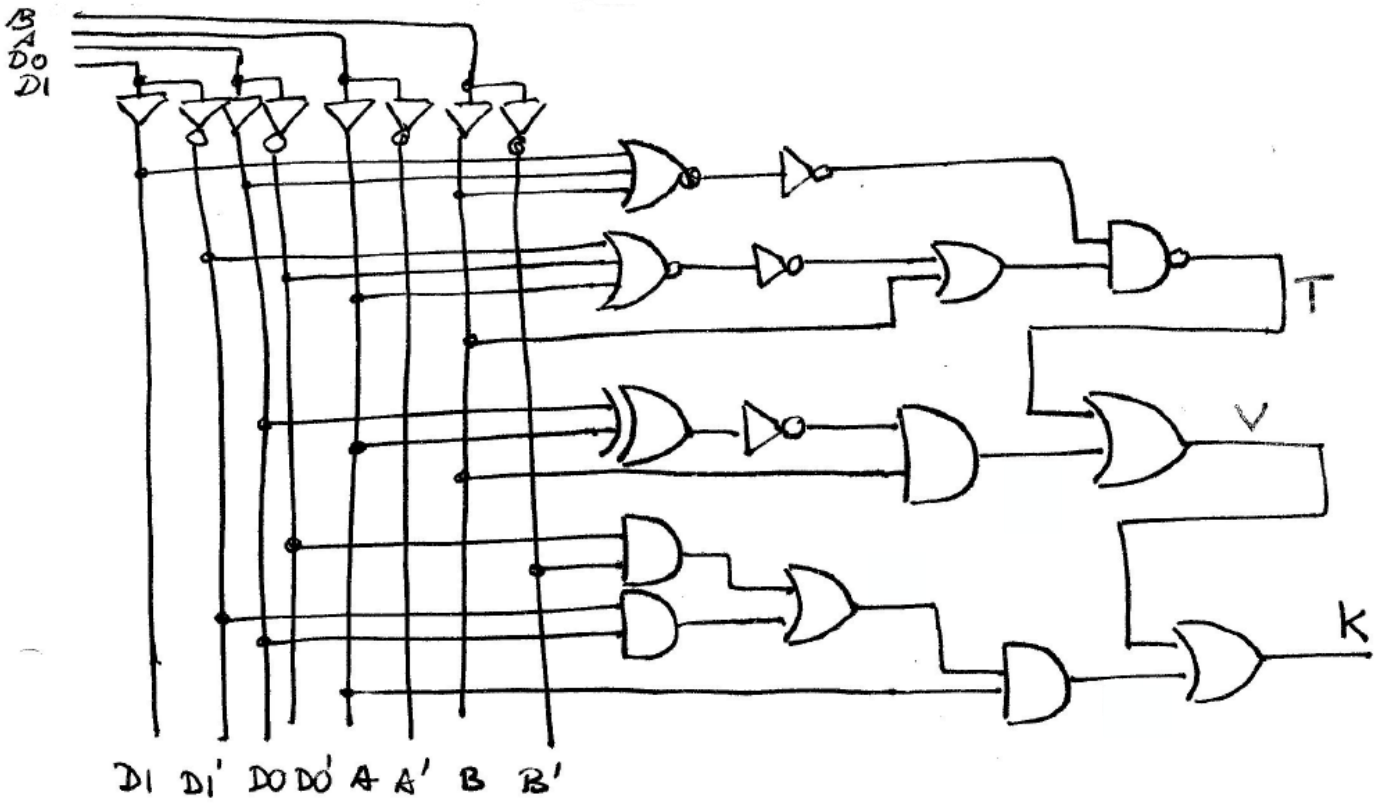
1.- Specifications

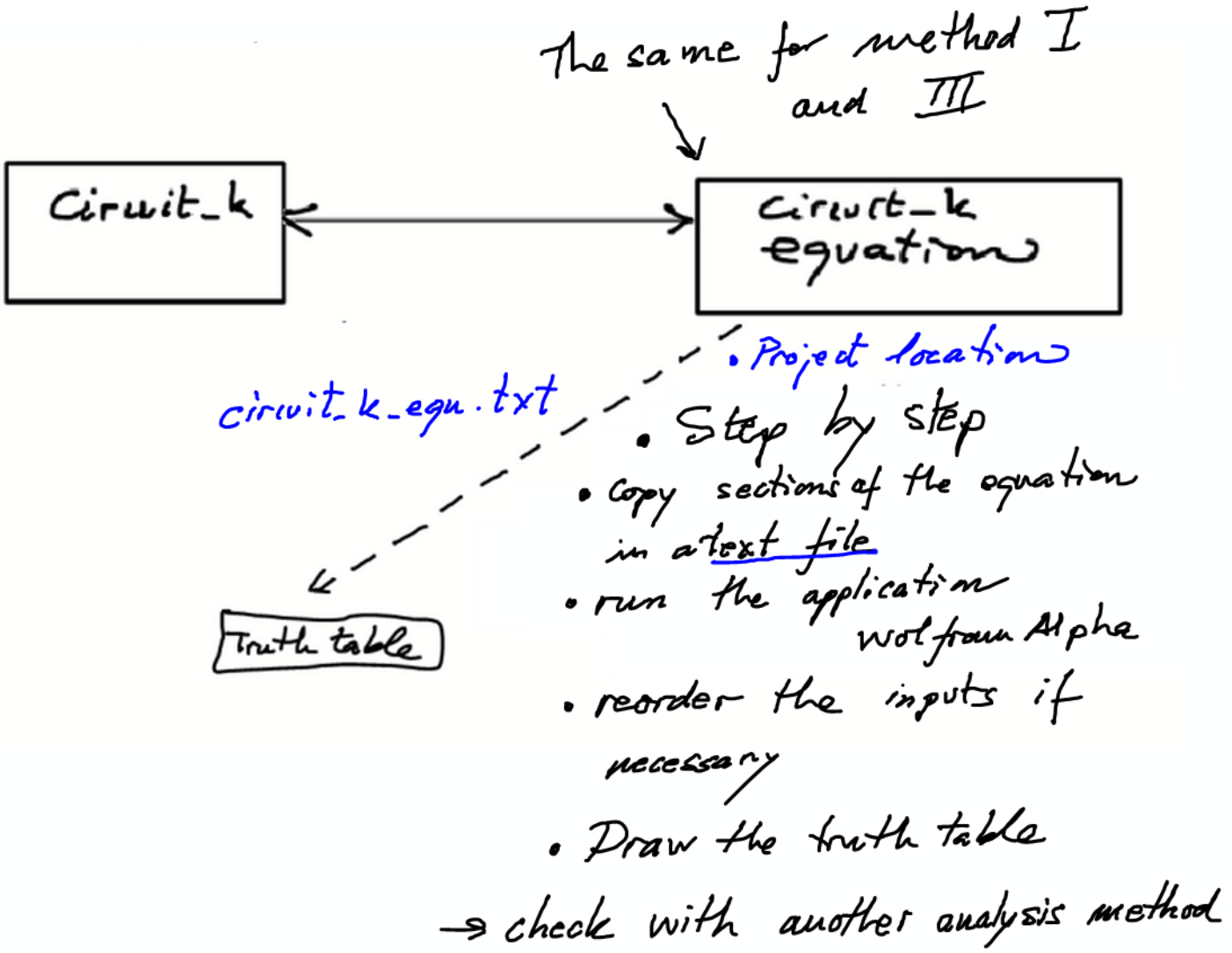
Find the truth table of the circuit_k using the method based on WolframAlpha (method IV)



Circuit internal architecture



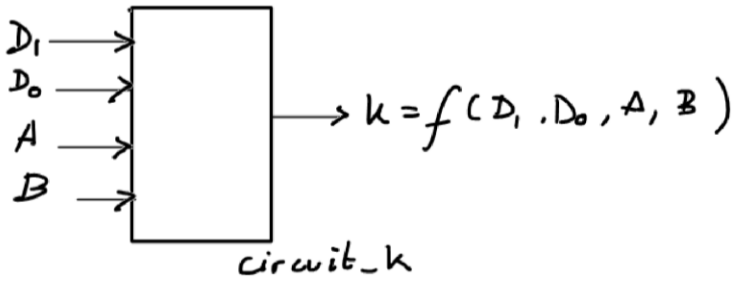
2.- Planning


The same for method I and III
Ciruit_k
Ciruit_k equation
• Project location
ciruit_k_equ.txt
• Step by step
• Copy sections of the equation in a text file
• run the application wolfram Alpha
• reorder the inputs if necessary
• Draw the truth table
Truth table
→ check with another analysis method

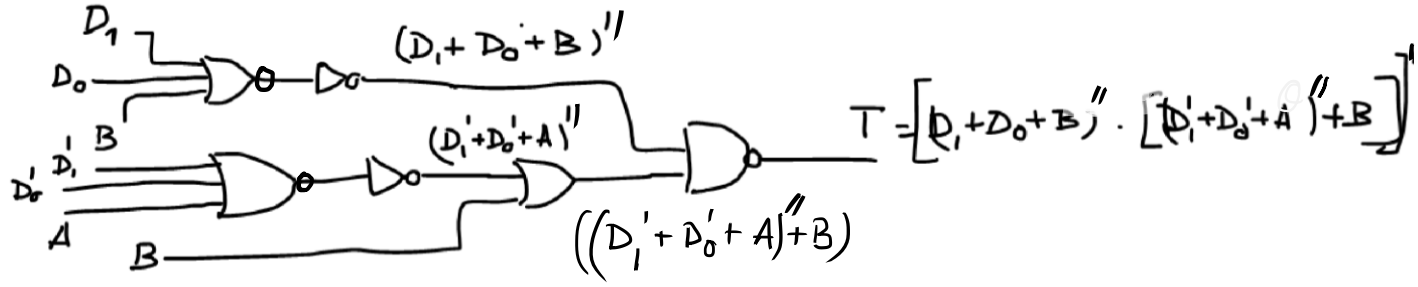
3.- Development

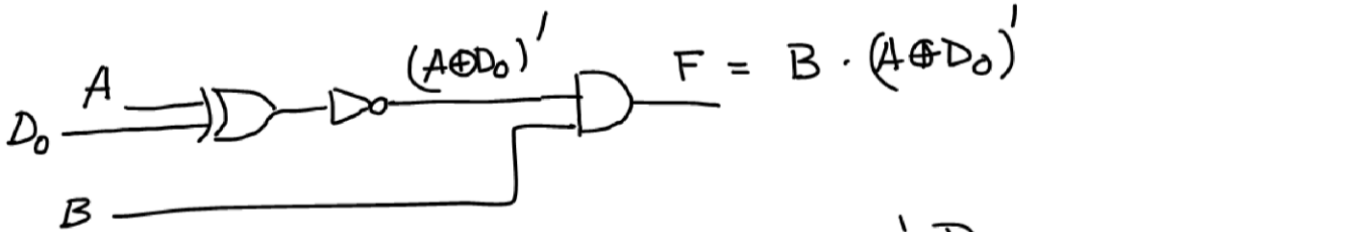
Obtain the circuit's equation

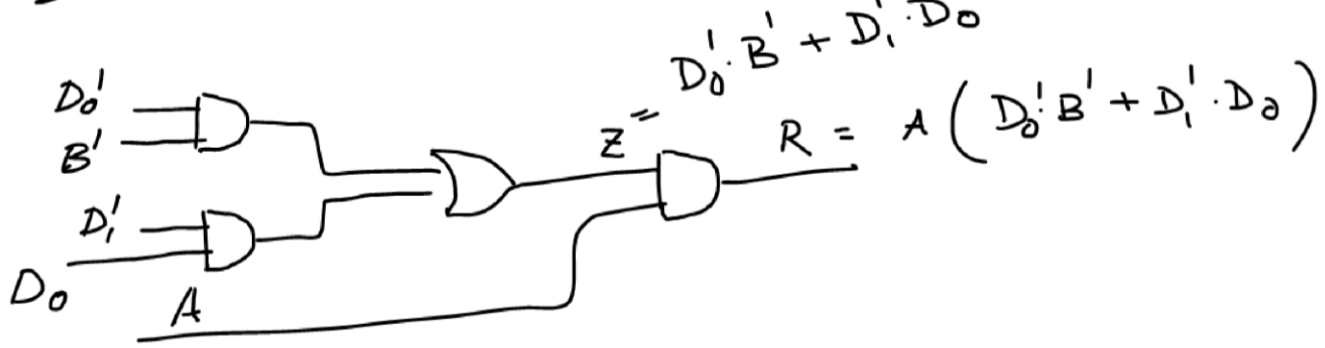
Expected solution

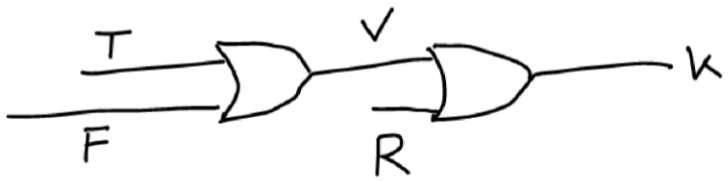


D_1	D_0	A	B	k
∅	∅	∅	∅	·
∅	∅	∅	1	·
⋮				
1	1	1	1	·









Finally: $k = R + V = R + (T + F) =$

$$\left[(D_1+D_0+B)'' \cdot \left[(D_1'+D_0'+A)'' + B\right]\right]' + \left[B \cdot (A \oplus D_0)'\right] + A \cdot \left[D_0'B' + D_1'D_0\right]$$

↗ Circuit_k equation

final

This is the circuit equation in WolframAlpha, (after several steps!)

also logic circuit

truth table not[[not(not(not(D1) or not(D0) or A)) or B] and not(not (D1 or D0 or B))] or [not(A xor D0) and B] or [(not(D0) and not(B) or not(D1) and D0) and A]

D1	D0	A	B	$\neg((\neg D1 \vee \neg D0 \vee A \vee B) \wedge (D1 \vee D0 \vee B)) \vee (\neg(A \veebar D0) \wedge B) \vee (((\neg D0 \wedge \neg B) \vee (\neg D1 \wedge D0)) \wedge A)$	
T	T	T	T	T	→ $m_{1111} = m_{15}$
T	T	T	F	F	
T	T	F	T	F	
T	T	F	F	T	→ $m_{1100} = m_{12}$
T	F	T	T	F	
T	F	T	F	T	→ $m_{1010} = m_{10}$
T	F	F	T	T	→ $m_{1001} = m_9$
T	F	F	F	F	
F	T	T	T	T	→ $m_{0111} = m_7$
F	T	T	F	T	→ $m_{0110} = m_6$
F	T	F	T	F	
F	T	F	F	F	
F	F	T	T	F	
F	F	T	F	T	→ $m_{0010} = m_2$
F	F	F	T	T	→ $m_{0001} = m_1$
F	F	F	F	T	→ $m_{0000} = m_0$

table interpretation

↳ $K = f(D_1, D_0, A, B) = \Sigma m(0,1,2,6,7,9,10,12,15)$

This is the truth table in sum of minterms

4. Test

We have solved the circuit using method I and also method IV and we obtain the same truth table with method III