Exam solution ideas

Problem 1

This is a solution of the circuit using method II: P1 analysis (method I). P1 in Proteus (method II) to check the analytical result and edited printed output waves.

If we zoom Chip1 low to high transition, we see that Chip0 and Chip1 are chained. The longest clock to output propagation path is CLK to Q1. If our FF are solved as standard FSM: $t_{CO\_MAX} = 2 \cdot t_{CO\_chip} = 2 \cdot (t_{CO\_FF} + 3 \cdot t_{P\_1gate})$

Problem 2

A similar circuit is D2.3. It is solved as a typical synchronous standard counter with six states with outputs in binary one-hot. See for example the *Counter_BCD_1digit* plan X example tutorial to repeat the design procedure step by step. Use Gray to encode the states (only 3 D_FF required).

For standard synchronous circuits designed systematically as FSM, their CLK to output propagation delay is predictable: $t_{CO\_FSM} = t_{CO\_FF} + 3 \cdot t_{P\_1gate}$

Problem 3

The CLK_Generator is a standard plan C2 circuit studied in L8.2. It consist of a chain of frequency dividers (*Freq_div_N*) and T_FF to square the output signals. Find the frequency dividers that generates the best approximation to the required frequencies: $N_1 = 182$; $N_2 = 9$; $N_3 = 2238$.

Higher accuracy requires finding better division ratios for each output frequency, thus an alternative circuit in our CSD course context may be based on a parallel internal architecture including three full frequency dividers and so many more *D_FF*.

Problem 4

How to chain shift registers is explained in L7.3. In this project two component will be required, a *Shift_reg_4bit* and a *Shift_reg_2bit*. The roulette project D2_12 option #3 uses a bit rotator based on shift registers.

Problem 5

How to chain standard radix-4 *Counter_mod16* is explained in L7.3. In this project two components will be required to reach the number 74. The roulette project D2_12 option #1 uses a modulo 37 counter based on *Counter_mod16.*

This counter expansion and count truncation mechanism is also explained for a modulo 24 in the highlighted project P7.

Problem 6

OSC and master reset circuits are discussed in L9.2. How to read inputs is presented in L9.3. How to write outputs is explained in, L9.4. The microcontroller pins that can be used as interrupts are discussed in this unit after having presented the FSM adaptation in L10.1:

Problem 7

A similar circuit is D3.3. Here we apply and adapt everything from the plan X solution of the *Counter_BCD_1digit* in LAB10 or also the serial transmitter highlighted in P10.

Problem 8

P12 design phase #1 example, as the first project proposed in the LAB11.

Problem 9

P12 design phase #2 and design phase #3 examples, as the second and third LAB11 projects. On the TMR0. Solving this project requires the planning in Problem 8.

Problem 10

Generating timing periods using TMR2 is presented as design phase#4 in the serial transmitter in P12. Solving this project requires the planning in Problem 8.