UPC. EETAC. Bachelor degree, Course 2A. Digital Circuits and Systems (CSD). Dr F. J. Robert. Grades will be available online on June 29th. Questions about the exam at office time.

Exam 2. **June 20th, 2022**

Problem 1. (2.5p)

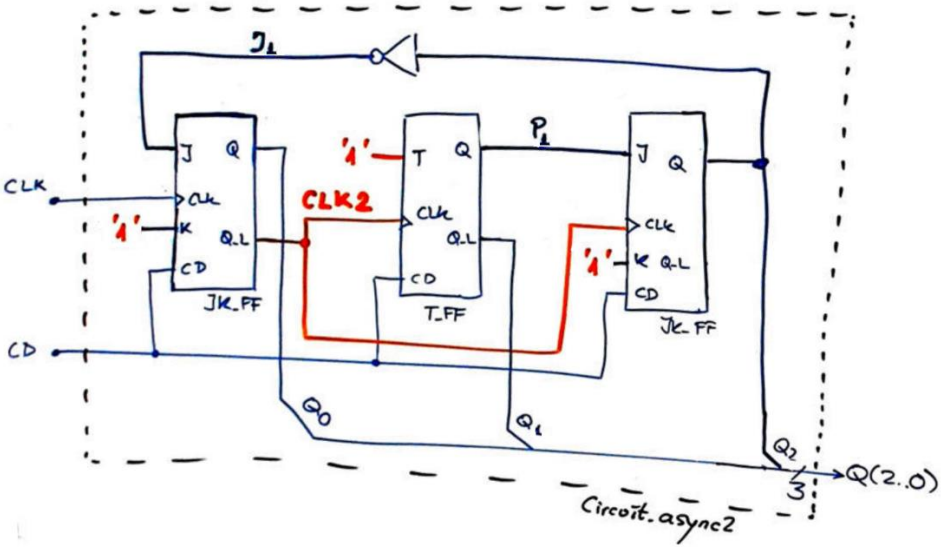


Fig. 1
Circuit based on 1-bit memory cells and combinational circuits.

1. Analyse the circuit in Fig. 1 to determine the output **Q(2..0)** completing an example timing diagram.
2. Explain why asynchronous circuits have disadvantages respecting synchronous circuits.
3. Explain how many VHDL files are necessary to develop and simulate the circuit using EDA tools.
4. If the propagation time of a logic gate is t_P = 4.2 ns, discuss and estimate the circuit's maximum speed.

Problem 2. (3.5p)

Let us design a synchronous two digits BCD modulo 37 [00, 01, 02, …, 09, 10, 11, …, 36, 00, 01, …] up and down counter for an electronic roulette as shown in Fig. 2. We will follow structural plan C2 using VHDL tools and counter chaining and truncation techniques using the standard *Counter_mod16* represented in Fig. 3 and other combinational components and logic. A decoder will translate BCD code to one-hot for driving high the 37 LED.

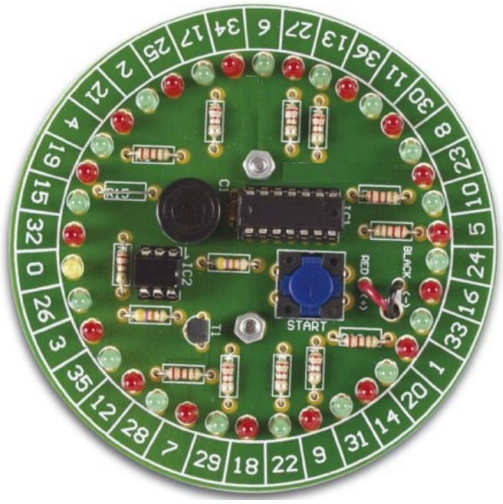
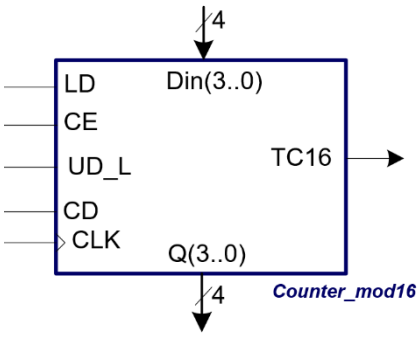


Fig. 2. Electronic roulette. The wheel have a zero (house edge), and numbers from 1 to 36. The odds of winning are thus 37 to one (2.7%).

1. Draw the top schematic of the application *roulette*.
2. Phase #1. Invent the units up counter [0, 1, 2, …, 8, 9, 0, 1, …] using count truncation.
3. Phase #2. Invent the BCD up counter modulo 37.
4. Phase #3. Enhance the previous design so that it can be reversible (up and down).



LD	CE	UD_L	Q^+	Synchronous operation after the CLK's rising edge
1	x	x	Din	Parallel load (register data)
0	0	x	Q	Do nothing (inhibit)
0	1	1	$(Q+1)_{mod16}$	Up counting in binary
0	1	0	$(Q-1)_{mod16}$	Down counting in binary

TC16 = '**1**' when CE = '1' *and* [(Q = 15 *and* UD_L = '1') *or* (Q = 0 *and* UD_L = '0')]; '0' otherwise

Fig. 3
Counter_mod16 symbol and function table.

Problem 3. (4p)

Design the interface for a portable CD player using a PIC18F4520 microcontroller as shown in Fig. 4.

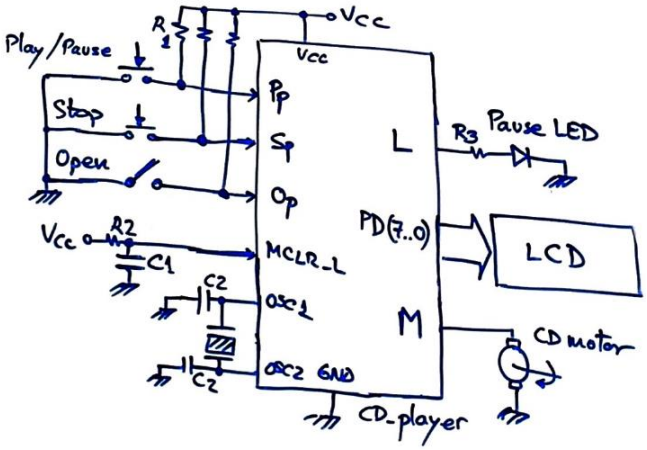


Fig. 4. CD player application and its symbol.

Quartz crystal oscillator frequency is 8 MHz.

1. Draw and explain the hardware-software diagram if we propose the FSM state diagram in Fig. 5 for running the application. Explain the difference between variables and flag variables.

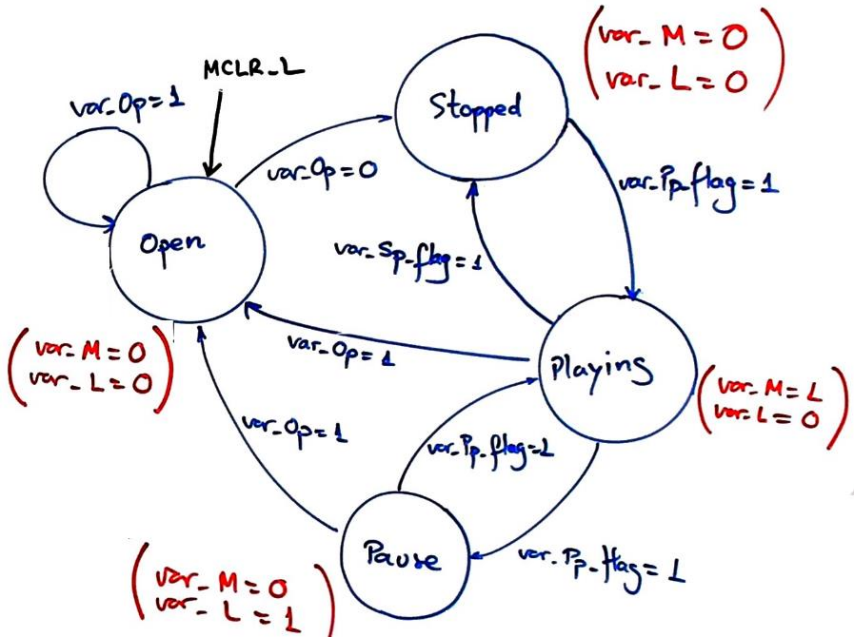


Fig. 5. CD player FSM state diagram.

2. Explain how to poll (read) the switch Open (Op) in *read_inputs()* connected to RC4 using bitwise operations. Explain how to measure how many times per second is this switch read.
3. The CD motor is connected at pin RB6. The pause LED is connected at pin RA2. Explain how to drive these outputs in *write_outputs().*
4. Explain the external interrupt mechanism for connecting Play/pause button at RB1/INT1 and Stop button at RB2/INT2 pin. Explain the general software flowchart for this application and how the *ISR()* is used.
5. Explain how to configure port pins and interrupts in *init_system().*
6. Draw the *state_logic()* truth table and its equivalent flowchart ready for translation to C language.
7. Explain how to connect and program the LCD display to show ASCII messages on the screen.
8. Configure and program TMR0 represented in Fig. 6 to generate a squared 2.5 Hz signal so the LED will be blinking intermittently when at *Stopped* state. Explain whether new states are required.

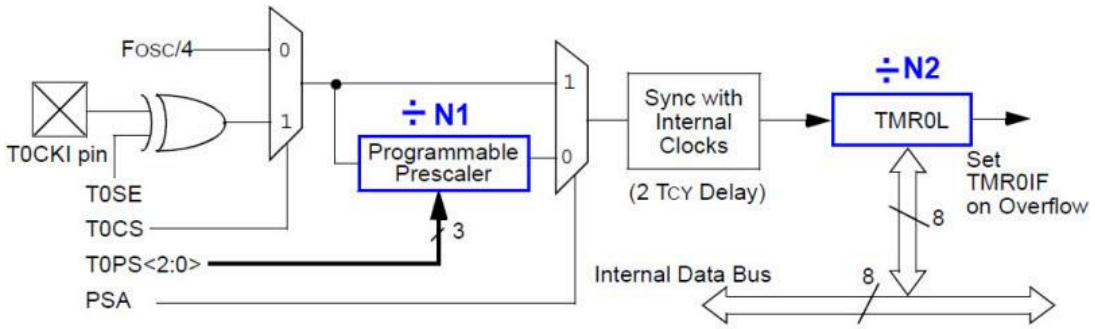


Fig. 6 TMR0 architecture for 8-bit mode.