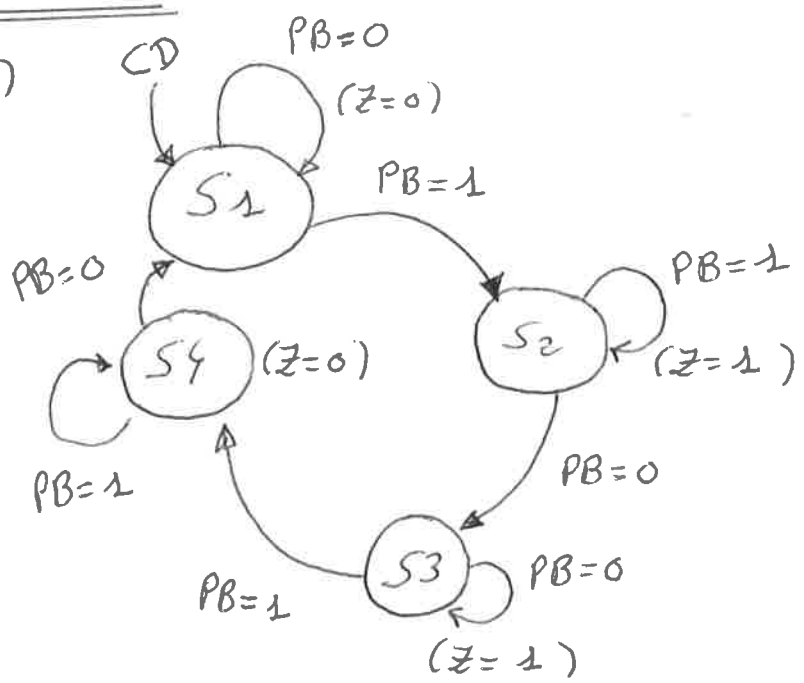
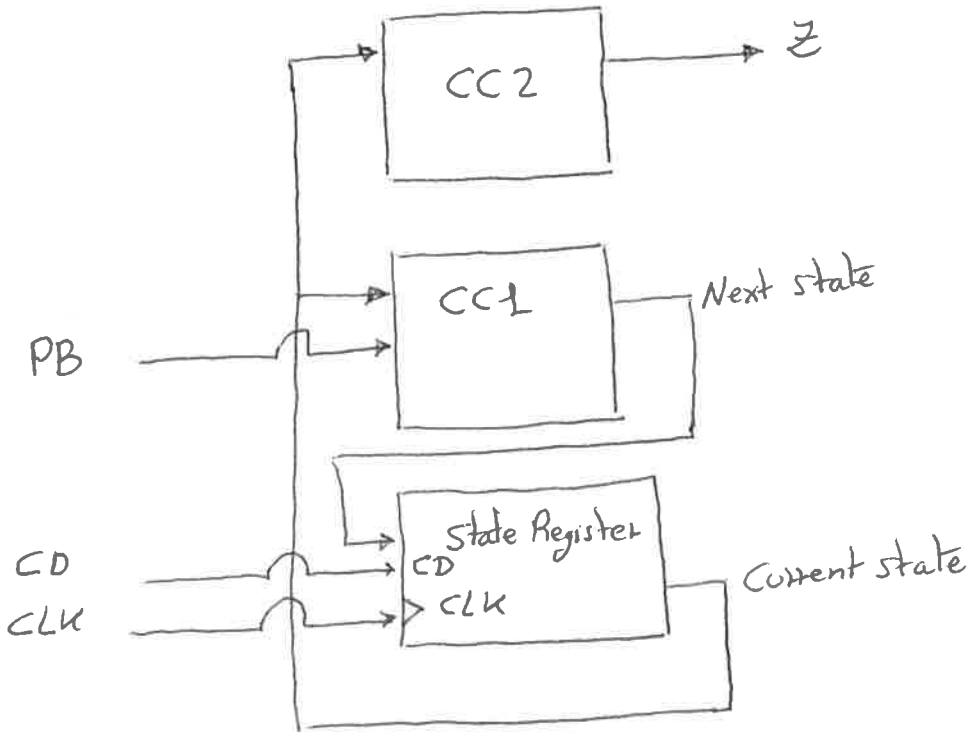
Problem 1

a)



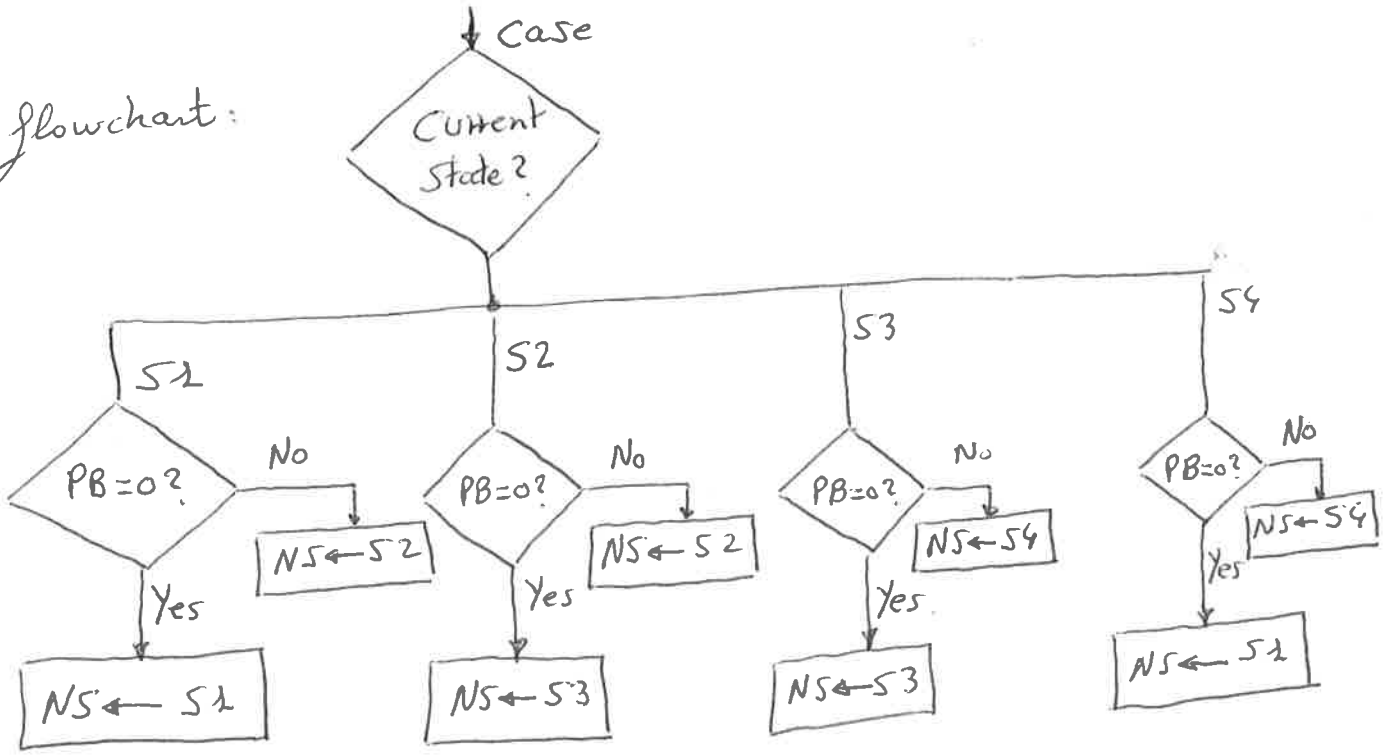
b) The state diagram has 4 states, then we need 2 D flip-flops. $= \frac{\log 4}{\log 2}$



c) CC1 truth table.

PB	Current state	Next state
0	S1	S1
1	S1	S2
0	S2	S3
1	S2	S2
0	S3	S3
1	S3	S4
0	S4	S1
1	S4	S4

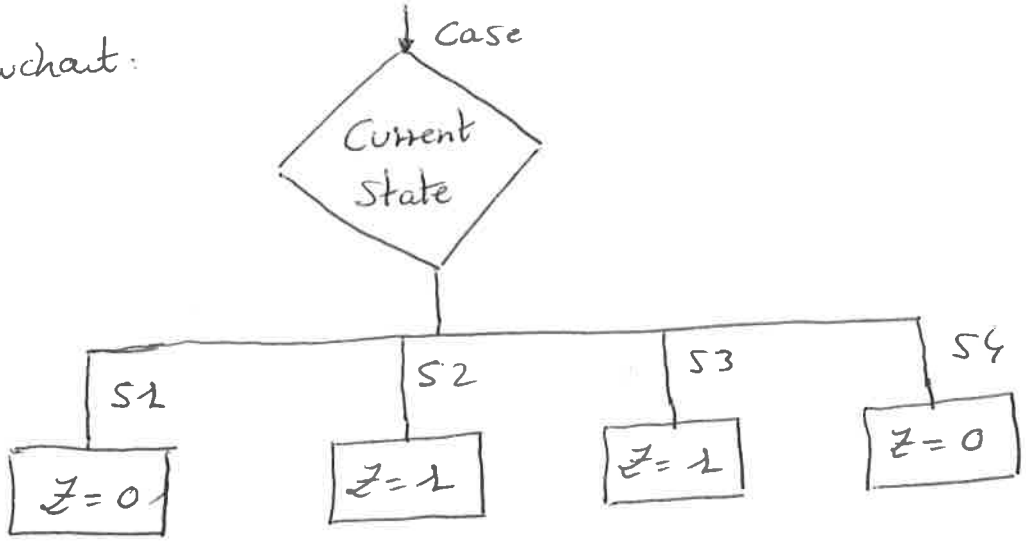
ASM flowchart:



d) CC2 truth table

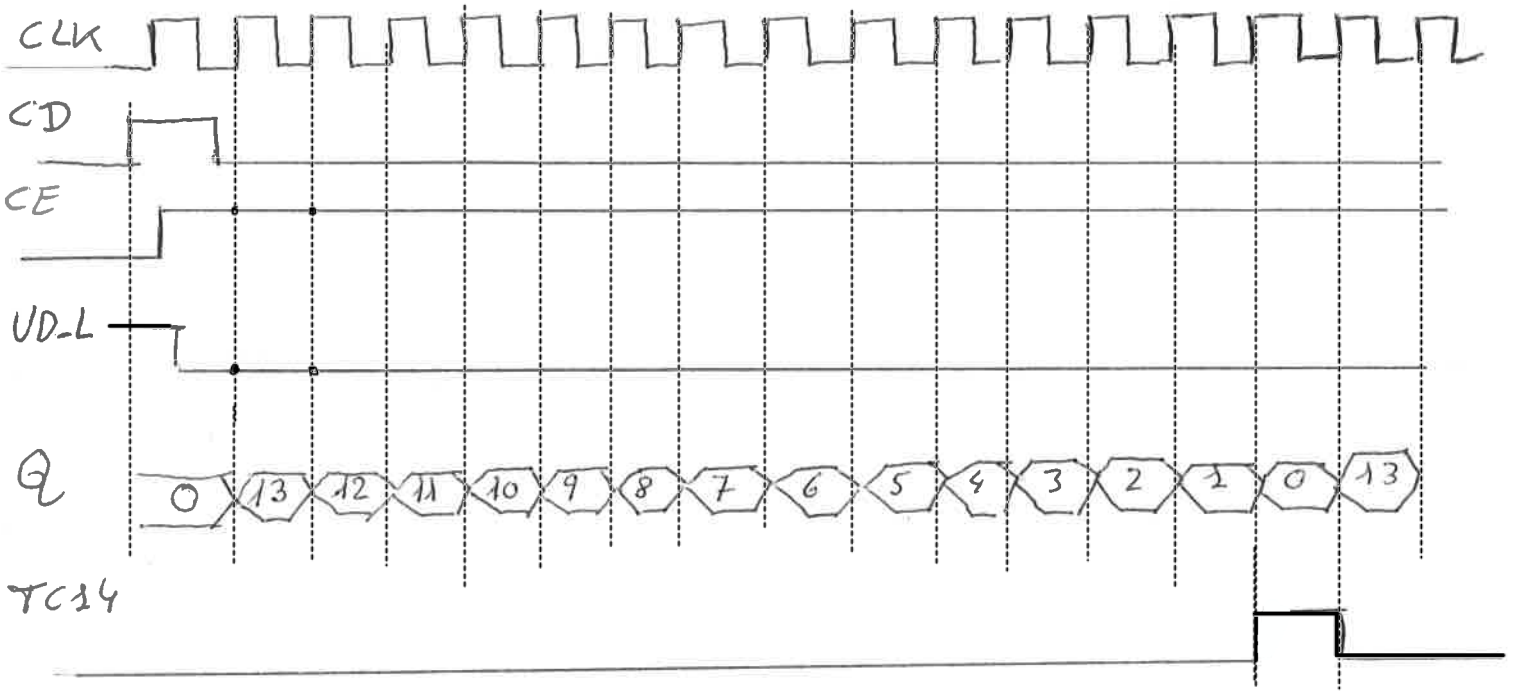
Current state	Z
S1	0
S2	1
S3	1
S4	0

ASM flowchart:

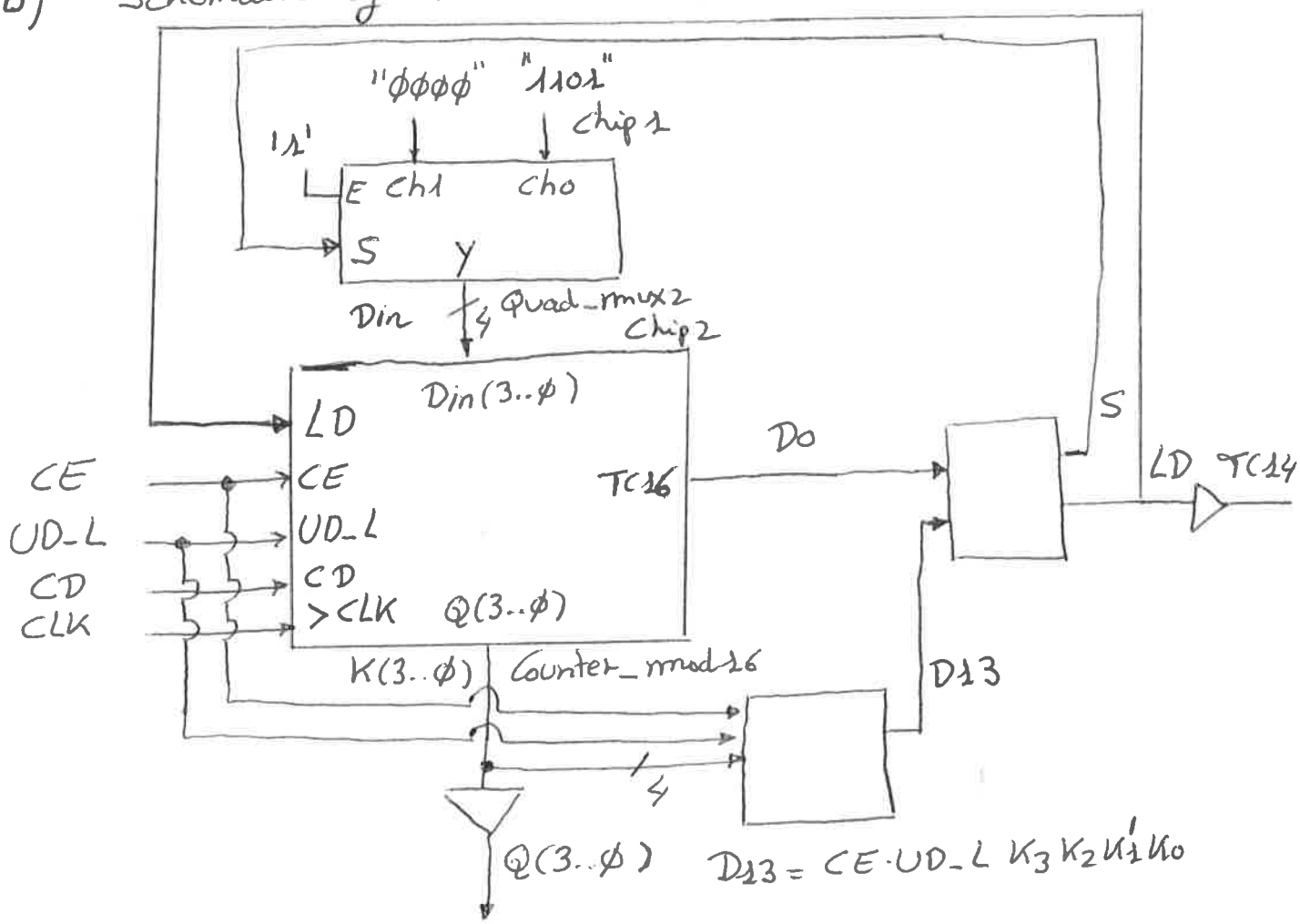


Problem 2

a)



b) Schematic of Counter_mod14



The multiplexer is used to select the truncating values, which are 0 and 13. These values are introduced to the input port Din(3..0) of the counter_mod16 by means of its LD input.

The counter_mod16 will include 4 D flip-flops, because its component counter_mod16 has 16 states.

c) The signals D0 and D13 are the inputs of the combinational circuit that implements the selection input (S) of the Quad-MUX2 and the LD input of the counter_mod16.

D0	D13	S	LD	
0	0	–	0	Counts
–	1	1	1	Jumps to 0
1	–	0	1	Jumps to 13

From this truth table we obtain:

$$S = D13$$

$$LD = D0 + D13$$

d) In this design there are 3 VHDL files involved: Quad_mux2.vhd, counter_mod16.vhd and the top design counter_mod16.vhd.

Counter_mod16 is organised using Plan Y, because it is much more practical than Plan X.